Bipolar LSI Data Book

Monolithic Memories

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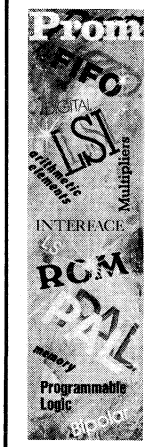

Second Edition

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Monolithic Memories MMI

Introduction

This book has been prepared to give the user a concise list of all Bipolar LSI Products offered by Monolithic Memories. It is divided by products into sections on HI REL, PROMs, ROMs, Character Generators, PAL, FIFO, Arithmetic Elements and Interface. Each section has been designed to allow the user the most useable format for the products described. The PROM, ROM, and Character Generator sections give data in the "generic" form allowing a quick review of the trade-off between devices. Cross references and selection guides are given where applicable. Programming and available programmers are given in detail. FIFO, PAL™, Arithmetic Elements and Interface data sheets are shown in detail for each product. This LSI data book was formatted with you, the user, in mind. For more information, contact the local Monolithic Memories sales representative or franchised distributor.

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Numerical Index

Monolithic Memories, Inc. is a company whose entire energies and resources are devoted to the development and production of Bipolar Large Scale Integrated (LSI) Memory and Logic circuits.

Since the company started its operation in 1970 the objective has been to establish its leadership in high-technology bipolar devices. Starting in 1971 MMI introduced the 1K PROM. This was followed with the first 2K PROM in 1972, the first 4K PROM in 1975 and the first 8K PROM in 1976.

In 1974 MMI started its expansion into the bipolar logic market with the introduction of the world's first 4-bit Slice, FIFO's Multipliers and most recently the Programmable Array Logic — PAL™.

Monolithic Memories is the world's leader in shipments of bipolar memory devices. The design fabrication and testing of all of our products is accomplished in a modern facility in Sunnyvale, California. Assembly of all devices is performed in a company owned facility in Penang, Malaysia. Both facilities are in the process of expansion to provide the bipolar LSI devices in great demand by the electronics industry.

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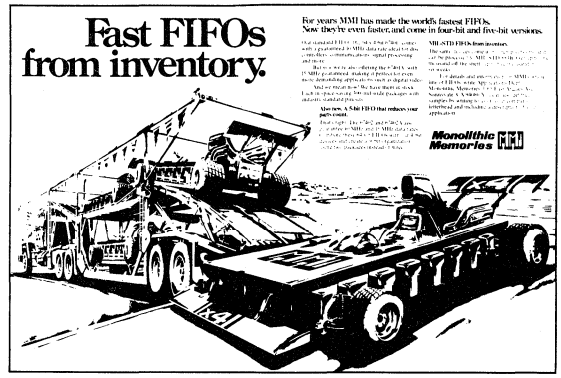
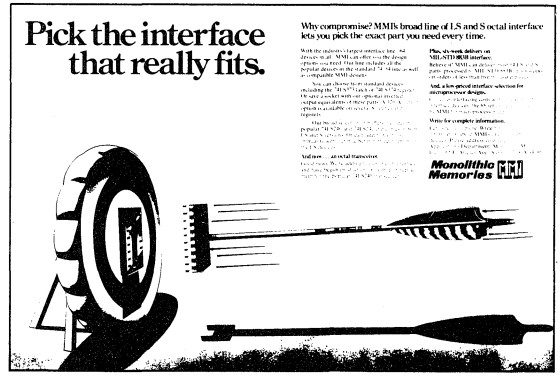


The company's products are used in a wide variety of products that range from electronic games to highly complex computer applications. There is a special emphasis placed on the manufacture of quality high-reliability devices for use in applications which include undersea and space programs.



Monolithic Memories sells its products through a worldwide organization of sales representatives and distributors in the United States, Europe and Japan.

Quality System

The quality system at Monolithic Memories is based on MIL-Q-9858, "Quality Program Requirements," MIL-I-45208, "Inspection System Requirements," and MIL-M-38510, Appendix A, "Product Assurance Program." MIL-M-38510 plays a significant role in structuring MMI's quality program.

MMI's facilities in Sunnyvale were certified in June of 1977 by DESC, Defense Electronics Supply Center, to manufacture and qualify to class B and class C Schottky Bipolar PROMs, ROMs and RAMs in accordance with the requirements of MIL-M-38510. This certification included a successful audit of our quality system to the stringent requirements of Appendix A of MIL-M-38510 which defines a Product Assurance Program tailored for integrated circuit manufacturers by DESC. This same quality system has also met the strict requirements of both "controlled" and "captive" line programs connected with our special Hi-Rel programs.

The quality accent at MMI is on process control as reflected in the use of many monitors and audits rather than gate inspections. This philosophy is consistent with building in quality and reliability rather than attempting to screen for it.

Process Control

MMI's advanced low-power Schottky TTL process uses such techniques as redundant masking to reduce random defects and self-aligning masking to reduce active chip area. Although more costly than the standard SSI or MSI Schottky TTL processes, these approaches yield better quality, increased reliability and lower overall cost due to higher net die per wafer. During the initial production stages of new designs and periodically thereafter, engineering characterizes the design-process compatibility by careful sample selection of lots reflecting process variable extremes.

Screening

Much of the assembly (packaging only) is performed offshore at our Penang, Malaysia facility. This facility has been qualified and is routinely monitored for conformance to MIL-STD-883 by MMI's military customers as well as by MMI's Quality Control Department. All standard military hermetic MMI products are 100% screened to MIL-STD-883 Class C. This includes:

- Pre-cap inspection.*
- High-temperature storage at 150°C.
- Temperature cycling. –65°C to +150°C.
- Constant acceleration.
- Fine and gross leak.
- Final electrical test.
- Q.A. sample acceptance testing.

*Modified for LSI.

Standard commercial hermetic product receives the following screens and monitors to insure the highest possible product quality.

- Pre-cap inspection*
- High temperature storage
- Temperature cycle
- Constant acceleration
- Fine and gross leak

} Daily monitors in lieu of 100% screening which insure the AQL levels before are met or exceeded.

- Final electrical test

*Modified MIL-STD-883 Pre cap.

The product assurance levels which MMI guarantees are listed in the table on this page.

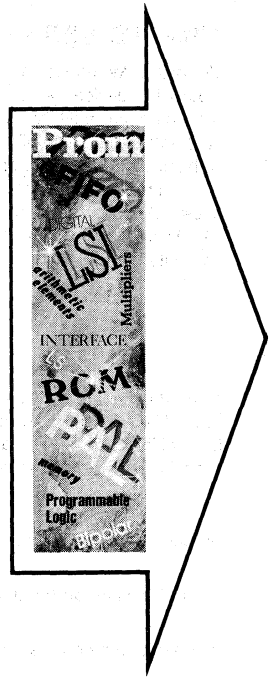
Reliability Engineering maintains product surveillance through routine sampling and submission to MIL-STD-883, method 5005, qualification testing. Additional step-stress and extended (limit) testing conditions are used when warranted. In general, failure rates have been found to be two orders of magnitude better than MIL-HDBK-217 estimates.

The quality organization is defined into three departments:

- Quality control
- Quality assurance
- Reliability assurance

Quality Assurance (AQL) Levels

TEST	LEVEL I COMMERCIAL (%)	LEVEL II MILITARY (%)
Hermeticity (includes fine and gross)	0.65	0.4
Electrical		
DC at 25°C	.40	.25
Functional at 25°C	.40	.25
AC at 25°C	.65	.40
DC at Temperature Extremes	.65	.65
Functional at Temperature Extremes	.65	.65
AC at Temperature Extremes	1.5	1.5



Hi-Rel Products

Hi-Rel Products

MMI's Hi-Reliability Program offers a broad line of industry standard Bipolar LSI components processed and tested to Military standards. All Hi-Reliability products can be purchased screened to Classes B or C of MIL-STD-883B, Method 5004, each with two options or in full compliance with MIL-M-38510 where slash sheets exist as delineated herein.

The inherent quality and reliability of MMI's products have been successfully demonstrated in such aircraft programs as F14, F15, F16, F18, MRCA and Mirage to name the most significant. We have supplied bipolar LSI devices for the Block V and Pioneer Venus Satellite programs.

Screening Options

The following process options are available:

MIL-M-38510 Class B

MIL-STD-883 Class B

MMI "B" Program (Includes Group A tests at 125°C; Group B requirements deleted)

MIL-M-38510 Class C

MIL-STD-883 Class C

MMI "C" Program (Includes Group A tests at 125°C, Group B requirements deleted)

Package Options

The package options available are:

J: Cerdip 16, 18, 20, 24 and 40 lead varieties standard.

D: Ceramic Sidebraze 16, 18, 24 and 40 lead upon request.

W: Ceramic Flatpack 16, 18 and 24 lead variety upon request.

F. Glass-metal Flatpack 16, 18 and 24 lead variety upon special request.

MIL-STD-883 Processed Parts

Monolithic Memories offers a complete line of high reliabilty bipolar LSI devices. All of our products are designed to operate over the entire military performance specification of ±10% V_{CC} tolerance and −55°C to +125°C operating temperature ambient. As such, all standard military temperature range devices can be processed either to full compliance of Classes B and C of MIL-STD-883 or to only the 100% screening criteria of MIL-STD-883 (Method 5004) for both Classes B and C (MMI equivalent) as delineated in Table 1.

Many deivces are available from stock. In addition to standard MIL-STD-883 high reliability devices, "Monolithic Memories has the ability to process parts to customers unique screening specifications. Some examples are:

- Selected electrical parameters
- 100% instant on (cold start) testing at −55°C
- Read and record data with Δ drift parameters
- Complete data reduction including mean, average, and three sigma analysis of each parameter
- Extended burn-in screening
- 100% AC, DC and functional testing at temperature extremes - -55°C and +125°C
- DPA (Destructive Physical Analysis)
- SEM (Scanning Electron Microscope) evaluation on a wafer lot basis.
- Special lot traceability to critical wafer fabrication processes, i.e., metalization
- Residual gas analysis on hermetic packages
- Custom lot qualification tests
- Special customer source inspection at pre-cap, SEM, process control monitoring points or at lot qualification testing

Table 1 Hi Rel Screening

MMI Available Standard Hi-Rel Screening Levels[c]

FLOW	METHOD	883C METHOD 5004[a]				MMI "C"[b]				883C METHOD 5004[a]				MMI "B"[b]			
		PROM/PAL		ROM/ HAL	LSI*	PROM/PAL		ROM/ HAL	LSI*	PROM/PAL		ROM/ HAL	LSI*	PROM/PAL		ROM/ HAL	LSI*
		Unpro-grammed	Pro-grammed			Unpro-grammed	Pro-grammed			Unpro-grammed	Pro-grammed			Unpro-grammed	Pro-grammed		
Pre-cap visual (prior to seal)	2010 Cond B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Seal		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
High Temp storage 24 Hr. @ 150°C (after seal)	1008 Cond. C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Temp. cycling 10 cycles, –65°C to +150°C	1010 Cond. C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Constant acceleration: Y_1 30 KG	2001 Cond. E	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Leak: Fine-5 x 10^{-8}cc/sec Gross—	1014 Cond. A or B 1014 Cond. C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Interim electrical test, DC & functional 25°C (correlated)	MMI Data Sheet	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Test fuse/verify (DC)	MMI Std.	Yes	Yes	—	—	Yes	Yes	—	—	Yes	Yes	—	—	Yes	Yes	—	—
Program/verify		—	Yes	—	—	—	Yes	—	—	—	Yes	—	—	—	Yes	—	—
Burn-in 160 hr. @ 125°C	1015 Cond. D (Dynamic)	—	—	—	—	—	—	—	—	—	Yes	Yes	Yes	—	Yes	Yes	Yes
Final Electrical Test Static Tests at 25°C	MMI Data Sheet	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
–55°C, +125°C		—	—	—	—	—	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
—Dynamic[d] & switching tests @ 25°C		—	—	—	—	—	—	—	—	—	Yes	Yes	Yes	—	Yes	Yes	Yes
—Functional Tests at 25°C		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Lot Acceptance: Group A Subgroup 2		—	—	—	—	Yes	Yes	Yes	Yes	—	—	—	—	Yes	Yes	Yes	Yes
Sub 1, 2, 3, 7, 8, 9 except Sub 9 for unprogrammed devices		Yes	Yes	Yes	Yes	—	—	—	—	Yes	Yes	Yes	Yes	—	—	—	—
Group B tests		Yes	Yes	Yes	Yes	—	—	—	—	Yes	Yes	Yes	Yes	—	—	—	—

[a] Tested in full accordance with MIL-STD-883 requirements

[b] Tested only to 100% screening requirements of MIL-STD-883 Method 5004. Reduced Group A testing and Group B testing not performed.

[c] MMI will screen and test to the latest issue in effect or as dictated by the contract.

[d] Dynamic Testing at 25°C, +125°C, –55°C; Switching tests at 25°C only.

* LSI Logic Products (include 54SXXX and 54LSXXX Interface circuits)

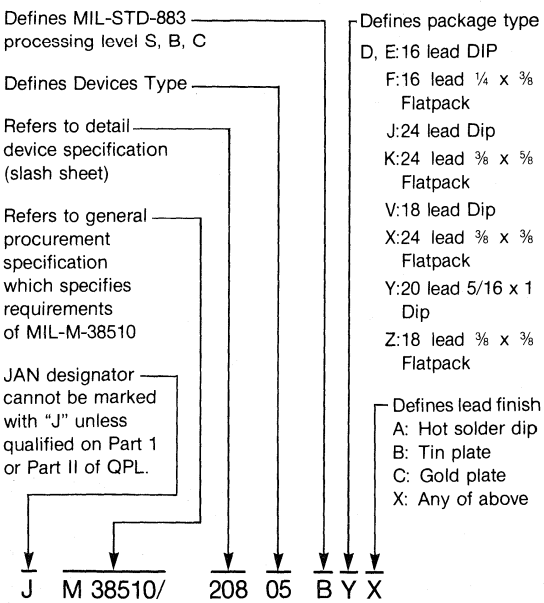
MIL-M-38510

The MIL-M-38510 Program is designed to standardize the Hi Reliability portion of the microcircuit industry much the same as MIL-S-19500 standardized the transistor industry. Its purpose is to provide the customer the highest possible quality level for the required application along with reasonable prices and fastest delivery.

The device electrical and package requirements of MIL-M-38510 are detailed by a device specification referred to as a slash sheet. Each slash sheet defines the microcircuit electrical performances and mechanical requirements. Each device listed on a slash sheet is referred to as a dash number and the group of microcircuits contained on a slash sheet is defined as a family of devices.

A unique MIL-M-38510 part number completely defines the microcircuit being procurred: Device type, electrical specification, mechanical outline, 100% screening requirement/quality level, and lead finish in the following format (Table 2).

Table 2: MIL-M-38510 Part Numbering Format



In addition, all MIL-M-38510 microcircuits must be completely manufactured and assembled in a domestic USA facility.

We have a strong committment to the MIL-M-38510 program and participate in slash sheet development with DESC, RADC and our customers. We have or will qualify all of our products for which there is a released MIL-M-38510 detailed specification (slash sheet). If one requires a product for which a slash sheet does not exist—then we can provide "883 processed" product. "883 processed" parts are screened to the full requirements of MIL-STD-883 Methods 5004 and 5005 with full electrical tests (DC, switching, and functional) over the military temperature range per MMI data sheet limits in our DESC certified facility. Each lot of 883 processed devices shipped includes a Certificate of Conformance and Group A Summary Report.

Currently released "slash sheets" for MMI supplied product are as follows:

MIL-M38510/203	1K Schottky NiCR PROMS (256x4)	01 5300-1 02 5301-1
MIL-M-38510/204	2K Schottky NiCR PROMS (512x4)	01 5305-1 02 5306-1
MIL-M-38510/206	4K Schottky NiCR PROMS (1kx4)	01 5352-1 02 5353-1
MIL-M-38510/207	1/4K Schottky NiCR PROMS (32x8)	01 5330-1 02 5331-1
MIL-M-38510/208	4K Schottky NiCR PROMS (512x8)	01 5340-1 02 5341-1 04 5348-1 05 5349-1
MIL-M-38510/209	8K Schottky NiCR PROMS (1Kx8)	03 5380-1 04 5381-1

For an up-to-date status on our QPL program, call your factory representative.

Advanced Programs

MMI has participated in the Trident Missile program since 1975. This participation has involved two manufacturing concepts for the production of Extreme Reliability Components.

1. Controlled Line—This concept places MMI manufacturing documentation and equipment under customer control and concurrence with any change.

2. Captive Line—This concept defines the equipment to be used, controls and supplies wire and packages. MMI documents the systems and provides the semiconductor expertise.

The Military Programs Department is involved in TRIDENT, DISCUSS, MX, F-18, MK500 and various NASA/SPACE PROGRAMS. Our products have the capability of meeting full radiation requirements of neutron, gamma dot and ionizing environments.

Our facility has DOD clearance and we have the capability to participate in customer analysis of our designs. These analyses may lead to design changes which enhance the product capability in hostile environments. Products which have been qualified for these advanced programs are:

5301—1K NiCR PROM
5300—1K Gold PROM
5341—4K NiCR PROM
5206—2K ROM (5306 NiCR PROM Equivalent)

Contact us for further details should you require this facet of our Hi-Reliability capability.

Flat/Pack Chip Carriers and Die

Most products are available in flat packs (see individual selection guides and the package appendix for details), and our manufacturing line can accommmodate your chip carrier packaging requirements as well. If your needs are for the ultimate in density, we can also supply LSI chips for your hybrid applications. These can be furnished with special 100% testing and optical inspection screens geared for hybrid packaging.

Ordering Information

Each of the screening options which MMI offers can be identified by a unique indicator for a given product. This part/screening identification system must be used when placing an order to ensure that the desired screening level is ordered. The product delivered is also marked with this indicator to verify compliance with purchase order requirements. Table 3 below provides the details of the screening identification system and includes an example.

In-House Reliability Programs

In addition to the execution of specific customer requested Hi-Rel testing, the Reliability Assurance Group conducts the following activities to establish and maintain our complete line of Hi-Reliability Bipolar LSI devices.

- Device design qualification (new/revised)
- Package qualification
- Process qualification
- On-going device/package/process qualification program.
- Extended and accelerated life testing (step/stress).
- Periodic reliability reports for in-house/field consumption.
- Process monitors (SEM).

2

Table 3 Screening Level Identification/Part Marking

SCREENING LEVEL	PRODUCT IDENTIFICATION	EXAMPLE USING 512x8 NiCR PROM WITH TRI STATE OUTPUTS AND ENCASED IN 20 PIN CERDIP
MIL-M-38510 Class B	MIL-M-38510/XXXXX BXX or JM38510/XXXXX BXX	JM38510/20805 BYX
MIL-STD-883 Class B	5XXX-1X883B*	5349-1J883B
MMI "B" Program	5XXX-1XB	5349-1JB
MIL-M-38510 Class C	MIL-M-38510/XXXXX CXX or JM 38510/XXXXX CXX	JM38510/20805 CYX
MIL-STD-883 Class C	5XXX-1X 883C	5349-1J883C
MMI "C" Program	5XXX-1XC	5349-1JC

*–1 identification for Schottky NiCR PROMS only.

Table 4 Group A Electrical Tests

SUBGROUPS	LTPD		INITIAL SAMPLE SIZE*	
	B	C	B	C
Subgroup 1—Static Tests at +25°C	5	5	45	45
Subgroup 2—Static Tests at Maximum Rated Operating Temperature	7	10	32	22
Subgroup 3—Static Tests at Minimum Operating Temperature	7	10	32	22
Subgroup 4—Dynamic Tests at +25°C†	5	5	45	45
Subgroup 5—Dynamic Tests at Maximum Rated Operating Temperature†	7	10	32	22
Subgroup 6—Dynamic Tests at Minimum Rated Operating Temperature†	7	10	32	22
Subgroup 7—Functional Tests at +25°C	5	5	45	45
Subgroup 8—Functional Tests at Maximum and Minimum Operating Temperatures	0	15	22	15
Subgroup 9—Switching Tests at +25°C Except Unprogrammed PROM	7	10	32	22

*Groups A, B, C, and D sampling plans are based on standard LTPD tables of MIL-M-38510 Appendix B. The smallest sample size based on zero rejects allowed, has been chosen unless otherwise indicated. If necessary, the sample size will be increased once to the quantity corresponding to the next acceptance number.

† Dynamic tests are not applicable to digital memory devices; switching subgroup tests are performed to a specified functional pattern and dynamically exercised.

Table 5 Group B Tests

TEST	METHOD	CONDITIONS	LTPD	INITIAL † SAMPLE SIZE
Subgroup 1 Physical Dimensions	2016	MMI Data Sheet	No failures	2
Subgroup 2 Resistance to Solvents	2015		No failures	4
Subgroup 3 Solderability	2003	Soldering temperature of +260°C ±10°C. 90% coverage, void concentration not to exceed 10% of area	15	15 Leads from 3 devices minimum
Subgroup 4 Internal Visual and Mechanical	2014	Failure criteria from design and construction	No failures	1
Subgroup 5 Bond strength	2011	Condition D: 3 gram force minimum for aluminum wire, ultrasonic bonding	15	15 wires from 4 devices minimum
Subgroup 6 Internal Water-Vapor Content* D-1-B	1018	100 ppm max. at +100°C	No failures 1 failure	3 5

*For packages with dessicant only. MMI packages do not contain a dessicant. Thus subgroup 6 does not apply.

† All samples are devices unless otherwise stated.

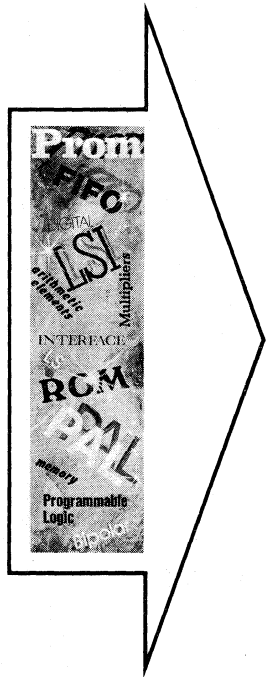
Table 6 Group C Tests (Die Related Tests)

TEST	METHOD	CONDITIONS	LTPD	INITIAL SAMPLE SIZE
Subgroup 1* Operating Life Test	1005	Steady state life: 1,000 Hr., +125°C, condition D, Dynamic	5	77 ACC = 1*
Subgroup 2* A. Temperature Cycling	1010	Test condition C: air to air, −65°C to +150°C, 10 cycles	15	15
B. Constant Acceleration (Centrifuge)	2001	Test condition E: 30kG centrifugal acceleration −Y_1 axis only		
C. Seal (Fine and Gross)	1014	Test Conditions A or B and C		
D. Visual Examination	1010			

Table 7 Group D Test (Packages Related Tests)

TEST	METHOD	CONDITIONS	LTPD	INITIAL SAMPLE SIZE
Subgroup 1 A. Physical Dimensions	2016	MMI Data Sheet	15	15
B. Internal Water Vapor Content	1018	5000 PPM max. @ 100°C	No failures 1 failure	3 5
Subgroup 2 A. Lead Fatigue	2004	Test condition: B_2: 3 oz. for ribbon leads: 8 oz. for all others	15	15
B. Seal (Fine and Gross)	1014	Test conditions A or B and C		
Subgroup 3* A. Thermal Shock	1011	Test method B: liquid to liquid, −55°C to +125°C, 15 cycles	15	15
B. Temperature Cycling	1010	Test condition C: air to air, −65°C to +150°C, 100 cycles		
C. Moisture Resistance	1004	Omit initial conditioning and vibration		
D. Seal (Fine and Gross)	1014	Test conditions A or B and C		
E. Visual examination	1004			
Subgroup 4* A. Mechanical Shock	2002	Test condition B: 5 shock pulses, 6 directions: 1500 g	15	15
B. Vibration Variable Frequency	2007	Test condition A: 20 g		
C. Constant Acceleration (Centrifuge)	2001	Test condition E: 30 kg centrifugal acceleration. Y_1 axis only		
D. Seal (Fine and Gross)	1014	Test conditions A or B and C		
E. Visual Examination	1010			
Subgroup 5 A. Salt Atmosphere (Corrosion)	1009	Test condition A: 24 Hr.	15	15
B. Seal (Fine and Gross)	1014	Test conditions A or B and C		
C. Visual Examination	1010			

* Electrical end points required for all subgroups (except in Group B and Subgroups 1, 2 and 5 of Group D), are room temperature. Subgroups 1, 2 and 3 of Group A DC tests, per MMI data sheet. Check factory for additional requirements.



Bipolar PROM Cross-Reference Guide

MEMORY DESCRIPTION				MMI	AMD	FAIR-CHILD	HARRIS	INTEL	INTERSIL	MOTOROLA	NATIONAL	RAYTHEON	SIGNETICS	TI
SIZE	ORGANIZATION	PINS	OUTPUT											
256	32x8	16	OC	**6330-1**	27S08/29750		7602		5600				N82S23	TBP18SA030 SN74S188
			TS	**6331-1**	27S09/29751		7603		5610				N82S123	TBP18S030 SN74S288
1024	256x4	16	OC	**6300-1**	29S10/29760		7610	3601	5603			29660	N82S27/82S126	TBP14SA10 SN74S387
			TS	**6301-1**	27S11/29761		7611	3621	5623			29661	N82S129	TBP14510 SN74S287
2048	256x8	20	OC	**6308-1**							DM74S470	29600		TBP18SA22 SN74S470
			TS	**6309-1**							DM74S471	29601		TBP18S22 SN74S471
		24	OC	**6335-1**										
			TS	**6336-1**										
2048	512x4	16	OC	**6305-1**	27S12/29770		7620	3602A	5604	MCM 7620	DM74S570	29610	N82S130	
			TS	**6306-1**	27S13/29771		7621	3602A	5624	MCM 7621	DM74S571	29611	N82S131	
4096	512x8	20	OC	**6348-1**			7648				DM74S473	29620		TBP18SA42 SN74S473
			TS	**6349-1**			7649				DM74S472	29621		TBP18S42 SN74S472
4096	512x8	24	OC	**6340-1**			7640	3604A	5605	MCM 7640	DM87S295	29624	N82S140	TBP18SA46 SN74S475
			TS	**6341-1**			7641	3624A	5625	MCM 7641	DM87S296	29625	N82S141	TBP18S46 SN74S474
4096	1024x4	18	OC	**6352-1**		93452	7642	3605	5606	MCM 7642	DM74S572		N82S136	
			TS	**6353-1**		93453	7643	3625	5626	MCM 7643	DM74S573		N82S137	
8192	1024x8	24	OC	**6380-1**		93450	7680	3608	5608	MCM 7680	DM87S229	29630	N82S180	TBP28SA86 SN74S479
			TS	**6381-1**		93451	7681	3628	5618	MCM 7681	DM87S228	29631	N82S181	TBP2S586 SN74S478

Note: Only commercial specification part numbers are listed.

AMD	MMI
27S08/29750	6330-1
27S09/29751	6331-1
27S10/29760	6300-1
27S11/29761	6301-1
27S12/29770	6305-1
27S13/29771	6306-1

FAIRCHILD	MMI
93450	6389-1
93451	6381-1
93452	6352-1
93453	6353-1

HARRIS	MMI
7602	6331-1
7603	6331-1
7610	6300-1
7611	6301-1
7620	6305-1
7621	6306-1
7648	6348-1
7649	6349-1
7640	6340-1
7641	6341-1
7642	6352-1
7643	6353-1
7680	6380-1
7681	6381-1

INTEL	MMI
3601	6300-1
3602A	6305-1
3602A	6306-1
3604A	6340-1
3605	6352-1
3608	6380-1
3621	6301-1
3624A	6341-1
3625	6353-1
3628	6381-1

INTERSIL	MMI
5600	6330-1
5603	6300-1
5604	6305-1
5605	6340-1
5606	6352-1
5608	6380-1
5610	6331-1
5618	6381-1
5623	6301-1
5624	6306-1
5625	6341-1
5626	6353-1

MOTOROLA	MMI
MCM 7620	6305-1
MCM 7621	6306-1
MCM 7640	6340-1
MCM 7641	6341-1
MCM 7642	6352-1
MCM 7643	6353-1
MCM 7680	6380-1
MCM 7681	6381-1

NATIONAL	MMI
DM74S470	6308-1
DM74S471	6309-1
DM74S472	6349-1
DM74S473	6348-1
DM74S580	6305-1
DM74S571	6306-1
DM74S572	6352-1
DM74S573	6353-1
DM87S228	6381-1
DM87S229	6380-1
DM87S295	6340-1
DM87S296	6341-1

RAYTHEON	MMI
29600	6308-1
29601	6309-1
29610	6305-1
29611	6306-1
29620	6348-1
29621	6349-1
29624	6340-1
29625	6341-1
29630	6380-1
29631	6381-1
29660	6305-1
29661	6306-1

SIGNETICS	MMI
N82S23	6330-1
N82S27/82S127	6300-1
N82S123	6331-1
N82S129	6301-1
N82S130	6305-1
N82S131	6306-1
N82S136	6352-1
N82S137	6353-1
N82S140	6340-1
N82S141	6341-1
N82S180	6380-1
N28S181	6381-1

TI	MMI
OLD NUMBERS	
SN74S188	6330-1
SN74S287	6301-1
SN74S288	6331-1
SN74S387	6300-1
SN74S470	6308-1
SN74S471	6309-1
SN74S472	6349-1
SN74S473	6348-1
SN74S474	6341-1
SN74S475	6340-1
SN74S478	6381-1
SN74S479	6380-1

TI	MMI
NEW NUMBERS	
TBP18SA030	6330-1
TBP14S10	6301-1
TBP18S030	6331-1
TBP14SA10	6300-1
TBP18SA22	6308-1
TBP18S22	6309-1
TBP18S42	6349-1
TBP18SA42	6348-1
TBP18S46	6341-1
TBP18SA42	6340-1
TBP28S86	6381-1
TBP28SA86	6380-1

Generic PROM Family
53/63XX-1

Features/Benefits

- **Standard Schottky processing**
- **Reliability proven nichrome fusible links (qualified for MIL-M-38510)**
- **PNP inputs for low input current**
- **Compatible pin configurations for upward expansion**
- **4-bit-wide and 8-bit-wide for byte oriented applications**

Application

- **Microprogram store**
- **Microprocessor program store**
- **Look up table**
- **Character generator**
- **Random logic**
- **Code converter**

Description

The 53/63XX-1-series generic PROM family offers the widest selection of sizes and organizations available in the industry. The 4-bit wide PROMs range from 256x4 to 1024x4 and feature upward/downward pin out compatibility in the space saving 16 and 18 pin packages. The 8-bit-wide PROMs range from 32x8 to 1024x8 in a wide selection of package sizes. All PROMs have the same programming specifications allowing a single generic programmer.

The family features low input current PNP inputs, full Schottky clamping, three-state and open collector outputs. The nichrome fuses store a logical high and are programmed to the low state. Special on chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high reliability.

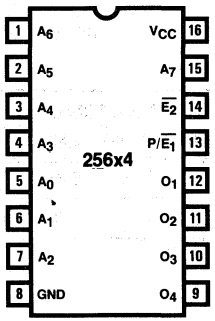
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Generic PROM Selection Guide

MEMORY			PACKAGE	DEVICE TYPE		
SIZE	ORGANIZATION			COMMERCIAL	MILITARY	
1K	256x4	OC	J16	6300-1	5300-1	4-bit-wide
		TS		6301-1	5301-1	
2K	512x4	OC	J16	6305-1	5305-1	
		TS		6306-1	5306-1	
4K	1024x4	OC	J18	6350-1	5350-1	
		TS		6351-1	5351-1	
		OC		6352-1	5352-1	
		TS		6353-1	5353-1	
1/4K	32x8	OC	J16	6330-1	5330-1	8-bit-wide
		TS		6331-1	5331-1	
2K	256x8	OC	J20	6308-1	5308-1	
		TS		6309-1	5309-1	
		OC	J24	6335-1		
		TS		6336-1		
4K	512x8	OC	J24	6340-1	5340-1	
		TS		6341-1	5341-1	
		OC	J20	6348-1	5348-1	
		TS		6349-1	5349-1	
8K	1024x8	OC	J24	6380-1	5380-1	
		TS		6381-1	5381-1	

Pin Configurations

53/6300-1
53/6301-1



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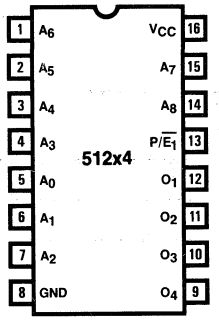

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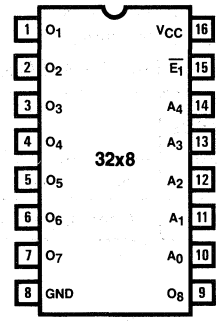
53/6331-1



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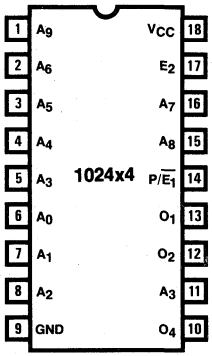

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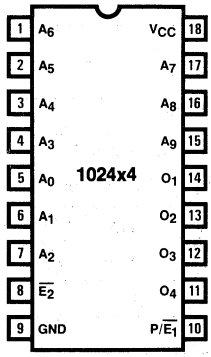

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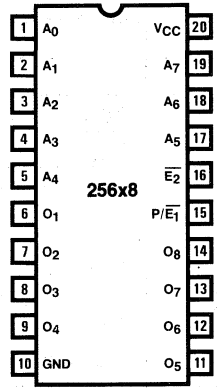

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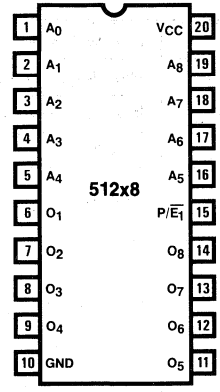

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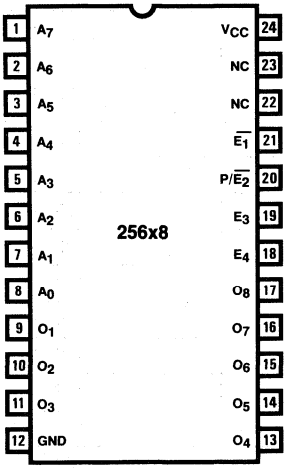
6336-1



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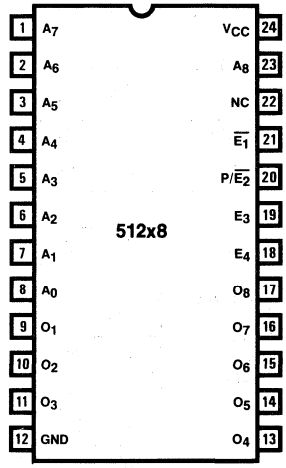

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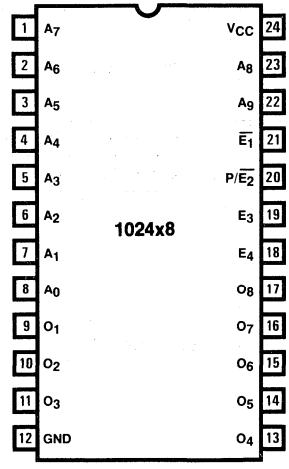


3

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA				–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V				–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 4.5V (Program Pin) V_I = V_{CC} MAX (Other inputs)				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OL} = 12mA	All PROMs except '30, '31, '80, '81			0.5	V
			COM I_{OL} = 16mA					
			MIL I_{OL} = 8mA	'30, '31, '80, '81				
			COM I_{OL} = 12mA					
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = –2mA		2.4			V
			COM I_{OH} = –3.2mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V				–100	μA
I_{OZH}			V_O = 2.4V				100	μA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V				100	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5V	V_O = 0V		–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded All outputs open	'30, '31				125	mA
			'00, '01, '05, '06				130	
			'08, '09, 6348/9				170	
			5348/9				155	
			'35, '36, '40, '41				170	
			'50, '51, '52, '53				175	
			6380/1				190	
			5380/1				180	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics

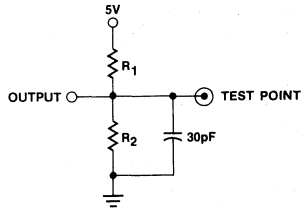
Over Commercial Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME	t_{EA} & t_{ER} (ns) ENABLE ACCESS & RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	R1(Ω)	R2(Ω)
6300-1, 6301-1	55	30	300	600
6305-1, 6306-1	60	30		
6308-1, 6309-1	70	30		
6335-1, 6336-1	70	30		
6340-1, 6341-1	70	30		
6348-1, 6349-1	70	30		
6350-1, 6351-1	60	30		
6352-1, 6353-1	60	30		
6330-1, 6331-1	50	30	375	750
6380-1, 6381-1	90	40		

Over Military Operating Conditions

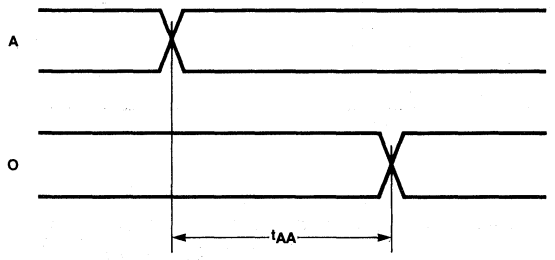
DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME	t_{EA} & t_{ER} (ns) ENABLE ACCESS & RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	R1(Ω)	R2(Ω)
5300-1, 5301-1	75	40	300	600
5305-1, 5306-1	75	40		
5308-1, 5309-1	80	40		
5335-1, 5336-1	80	40		
5340-1, 5341-1	80	40		
5348-1, 5349-1	80	40		
5350-1, 5351-1	75	40		
5352-1, 5353-1	75	40		
5330-1, 5331-1	60	40	375	750
5380-1, 5381-1	125	40		

Standard Test Load

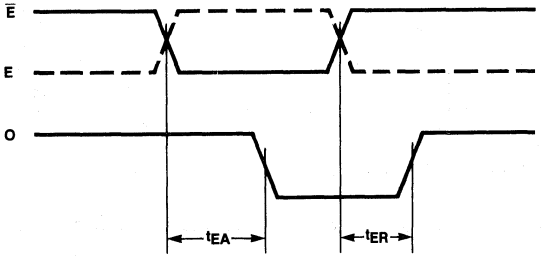


Input Pulse: 0V to 3V
Input Rise and Fall Times: 5ns from 1V to 2V
Measurements Made at 1.5V

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

PROM Programming Instructions
53/63XX-1

Description

The 53/63XX-1 Generic PROM Family is manufactured with outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be opened. This procedure is called programming.

Programming Procedure (See Figure 1)

1. Apply the desired address to the inputs.
2. Enable Inputs may be left at any state.*
3. Apply 5.5V to V_{CC}.
4. Apply V_{PP} to the program pin. (This step is not used on the 32x8 PROM)*.
5. Apply V_{OUT} to the output to be programmed. (Program only one output at a time).
6. Remove V_{OUT}.
7. Remove V_{PP}.
8. Verification may be performed after each bit or word or after completing the programming of all memory locations.

*The 5330/1 and 6330/1 do not have a program pin. For these devices the output only is used in programming a particular selected bit and the device must be in the disabled state.

Verification Procedure (See Figure 2)

1. Enable the device.
2. To verify low-state:
   - 2A. Apply an address where the output should be low.
   - 2B. Apply 4.2V to V_{CC}.
   - 2C. Load the output with I_{OL} = 12 mA.
   - 2D. Check that the output is less than 0.8V.
3. To verify High-state:
   - 3A. Apply an address where the output should be high.
   - 3B. Apply 6V to V_{CC}.
   - 3C. Load the output with I_{OH} = 0.3 mA.
   - 3D. Check that the output is higher than 4.5V.

Programming Parameters Do not test these parameters or you will program the device.

SYMBOL	PARAMETER	CONDITIONS TA = +25° C	FIGURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_R	Slew rate of Programming Pulses†			0.3		0.5	V/μs
V_{CCP}	VCC During Programming			5.4	5.5	5.6	V
	Maximum Duty Cycle					25	%
V_{PP}	Programming Voltage on Program Pin*		1	27		33	V
V_{OUT}	Programming Voltage on Output Pin*		1	20		26	V
t_{D1}	Delay between VPP and VOUT		1	0	10	20	μs
t_{D2}				0	0.5	1	
t_p	Pulse width of V_{OUT}		1	10		25	μs
V_{OLV}	VOL during verification	Chip enabled IOL = 12 mA VCC = 4.2V	2			0.8	V
V_{OHV}	VOH during verification	Chip enabled IOH = 0.3 mA VCC = 6V	2	4.5			V

*Voltage supply must be capable of supplying at least 240 mA.

†Leading edge of VPP and VOUT

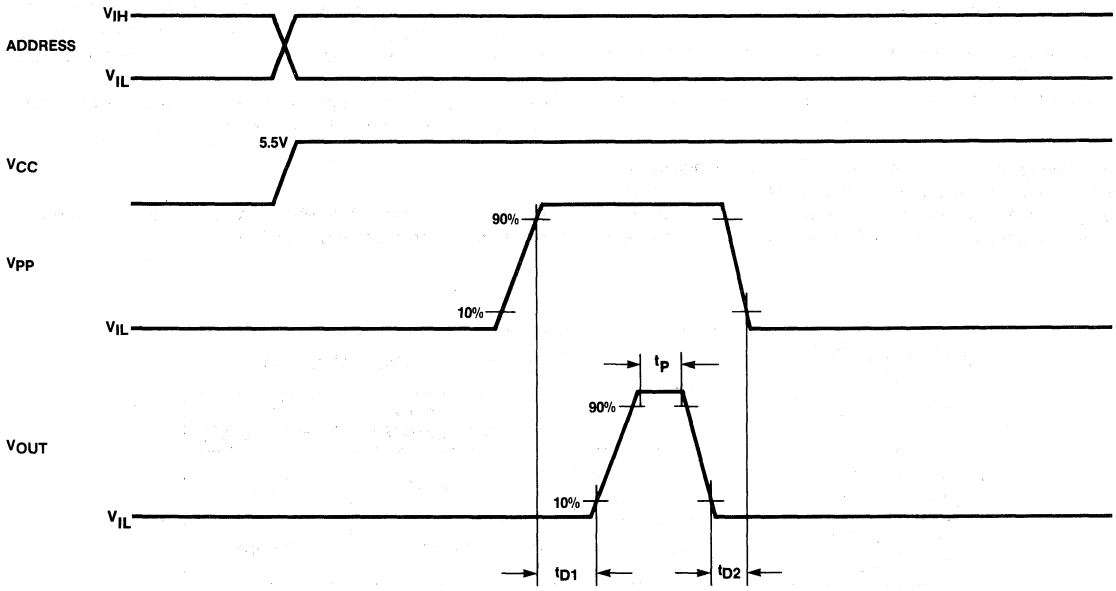


Figure 1. Programming Timing Diagram

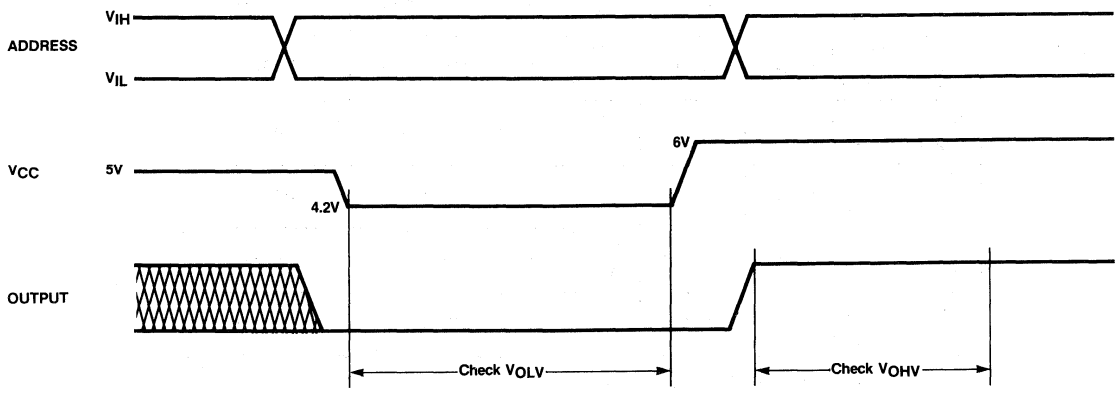


Figure 2. Verification Timing Diagram

Optimized Programming Algorithm

1. Pulse all fuses to be programmed with single, minimum voltage programming pulses (line 1 in the table).
2. Verify all fuses at low VCC (4.2V). During this step, unprogrammed fuses are pulsed up to eight more times (see table).
3. Re-verify at low VCC (4.2V) and high VCC (6V).

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27V	20V
4 to 6	30V	23V
7 to 9	33V	26V

Commercial Programmers

MMI PROMs are designed and tested to give a programming yield greater than 95%. If your programming yield is lower, check your programmer. It may not be properly calibrated. (See figures 1 and 2).

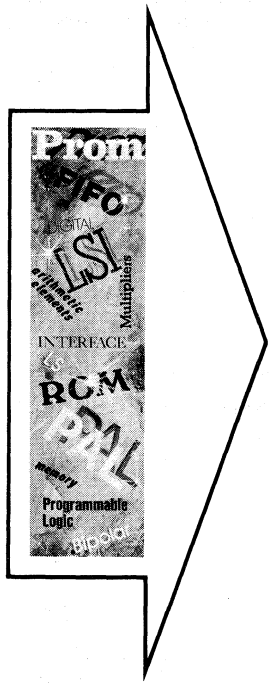
Programming is final manufacturing—it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. The best method involves a storage scope, with DC current probes clamped over the external wires to the program pin and the output pin. The current should not be limited at a value less than 240mA. This can be checked by using a 50-ohm resistor as a load. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember—The best PROMs available can be made unreliable by improper programming techniques.

PART NUMBER		SIZE	CONFIG.	OUT PUT	NO. OF PINS	SOCKET ADAPTER	
M	C					DATA I/O (ALL SERIES)*	PRO-LOG (SERIES 90, 92)†
5330-1 5331-1	6330-1 6331-1	1/4K	32x8	OC TS	16	715-1046	PA16-2
5300-1 5301-1	6300-1 6301-1	1K	256x4	OC TS	16	715-1035-1	PA16-1
5305-1 5306-1	6305-1 6306-1	2K	512x4	OC TS	16	715-1035-2	PA16-1
5308-1 5309-1	6308-1 6309-1	2K	256x8	OC TS	20	715-1028-1	PA20-2
5335-1 5336-1	6335-1 6336-1	2K	256x8	OC TS	24	715-1033-1	PA24-1
5340-1 5341-1	6340-1 6341-1	4K	512x8	OC TS	24	715-1033-2	PA24-1
5348-1 5349-1	6348-1 6349-1	4K	512x8	OC TS	20	715-1064	PA20-2
5350-1 5351-1	6350-1 6351-1	4K	1024x4	OC TS	18	715-1036	PA18-1
5352-1 5353-1	6352-1 6353-1	4K	1024x4	OC TS	18	715-1039-3	PA18-2
5380-1 5381-1	6380-1 6381-1	8K	1024x8	OC TS	24	715-1033-3	PA24-1

* Program card set is 909-1226-1 for all series DATA I/O

† Personality module is PM 9037 for all PRO-LOG (series 90, 92)



Generic ROM Family
52/62XX-1 52/62XX-2

Features/Benefits

- High bit density up to 16K
- PNP inputs for low input current
- High speed Schottky technology
- Open collector or three state outputs

Applications

- Character generator
- Look up table
- Microprocessor program store
- Microprogram store
- Random logic
- Code converter

Description

The 52/6200 series generic ROM family is available in sizes from 8K through 16K bits. The 8-bit-wide ROMs are available as 1Kx8 and 2Kx8 organization. Additional 9-bit and 10-bit-wide output configurations are available for custom logic or character generator applications.

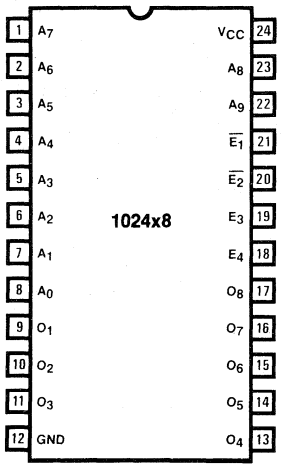
Generic ROM Selection Guide

MEMORY			PACKAGE	DEVICE TYPE	
SIZE	ORGANIZATION			COMMERCIAL	MILITARY
8192	1024x8	OC	J24	6280-1	5280-1
		TS		6281-1	5281-1
		OC		6280-2	5280-2
		TS		6281-2	5281-2
		OC		6282-1	5282-1
		TS		6283-1	5283-1
9216	1024x9	OC	J24	6260-1	5260-1
		TS		6261-1	5261-1
10240	1024x10	OC	J24	6255-1	5255-1
		TS		6256-1	5256-1
10368	1152x9	OC	J24	6290*	5290*
		TS		6291*	5291*
16384	2048x8	OC	J24	6275-1	5275-1
		TS		6276-1	5276-1

*Detailed information in section 5 (character generators)

Pin Configurations

52/6280-1 52/6280-2 *52/6282-1
52/6281-1 52/6281-2 *52/6283-1



*"OR" ENABLE = $\overline{E1}$ $\overline{E2}$ + E3 E4

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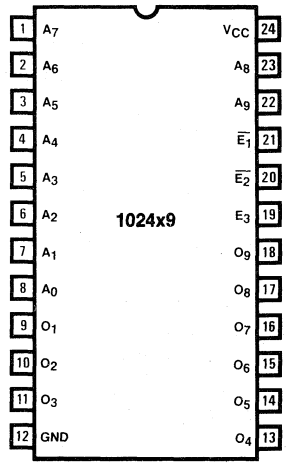
52/6261-1



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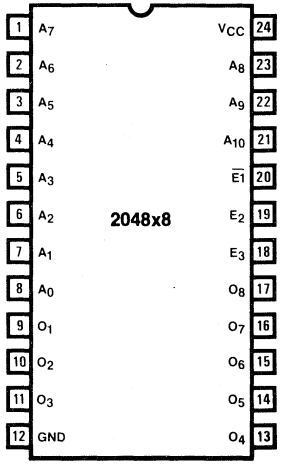

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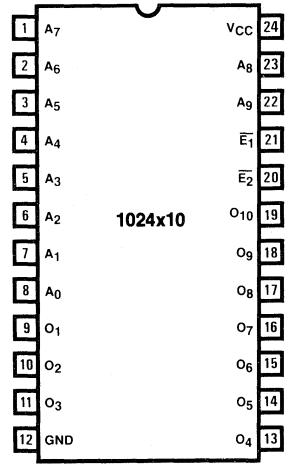


4

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA				–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V				–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				40	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1.0	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OL} = 8mA	'75, '76, '80, '81, '82, '83			0.5	V
			COM I_{OL} = 10mA					
			MIL, COM I_{OL} = 6mA	'55, '56, '60, '61				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = –1mA		2.4			V
			COM I_{OH} = –2mA					
I_{OZL}	Off-state output current	V_{CC} = MAX, V_O = 0.5V	'80, '81, '82, '83, '55, '56, '60, '61				–50	μA
			'75, '76				–100	
I_{OZH}		V_{CC} = MAX, V_O = 2.4V	'80, '81, '82, '83, '55, '56, '60, '61				50	μA
			'75, '76				100	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V				100	μA
I_{OS}	Output short-circuit current	V_{CC} = 5.0V	V_O = 0V		–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs grounded, All outputs open	'55, '60				165	mA
			'56, '61				175	
			'80, '82				170	
			'81, '83				180	
			'75, '76				190	

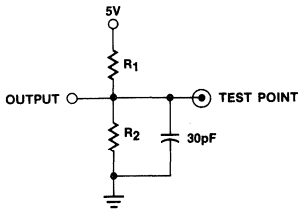
Switching Characteristics

Over operating conditions

DEVICE TYPE	t_{AA}(ns) ADDRESS ACCESS TIME	t_{EA}(ns) ENABLE ACCESS TIME	t_{ER}(ns) ENABLE RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	MAX	$R_1\Omega$	$R_2\Omega$
6255-1, 6256-1	100	70	40	750	1500
5255-1, 5256-1	150	80	45		
6260-1, 6261-1	100	70	40		
5260-1, 5261-1	150	80	45		
6275-1, 6276-1	110	40	40	560	1100
5275-1, 5276-1	120	50	50		
6280-1, 6281-1	100	70	45		
5280-1, 5281-1	175	90	50		
6280-2, 6281-2	55	30	30		
5280-2, 5281-2	75	35	35		
6282-1, 6283-1	100	70	45		
5282-1, 5283-1	175	90	50		

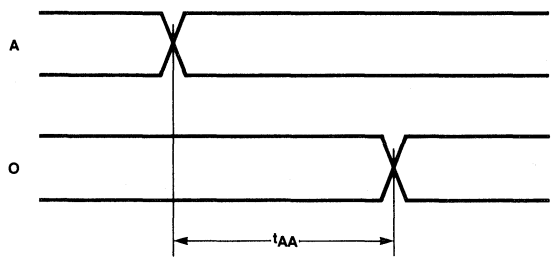
4

Standard Test Load

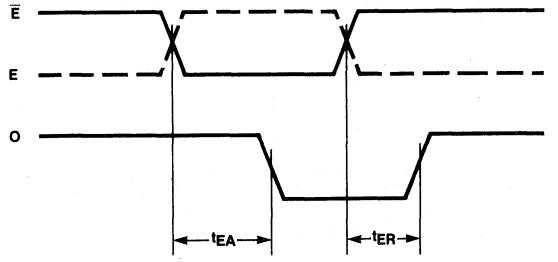


Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V

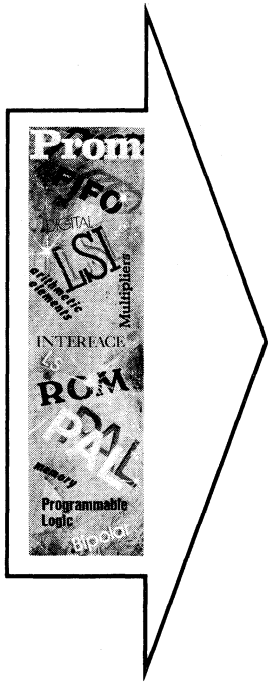
Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time



High Speed Character Generators

Features/Benefits

- 100 ns max. access time
- Low power dissipation—500 mW
- Standard packaging—18 pin dip/24 pin dip
- Single 5 volt supply
- 64/128 characters in one package
- Open collector or three-state

Applications

- CRT displays
- Printing calculators
- LED arrays
- Typesetting

Description

The intended application for these devices is the generation of 64 or 128 ASCII alpha-numeric characters utilizing a read out system which generates the characters either horizontally or vertically, one word line at a time.

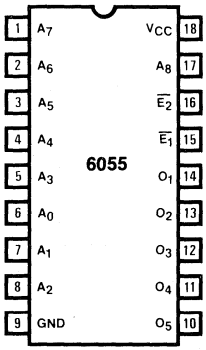
Character Generator Selection Guide

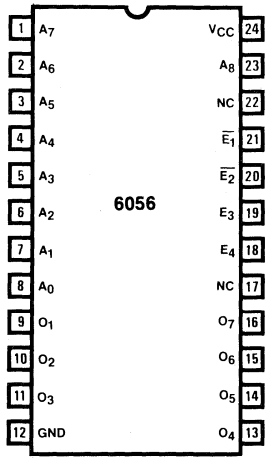
GENERIC PART NO.	CHARACTERS NO.	CHARACTERS TYPE	MATRIX	SCAN	COMMERCIAL OC	COMMERCIAL TS	MILITARY OC	MILITARY TS	PKG
6055	64	ASCII	5 x 7	Row	6055	6155	5055	5155	J18
6056 †			5 x 7	Column	6056	6156	*	*	J24
6071			7 x 9	Row	6071	6171	*	*	J24
6061 †	128	ASCII	5 x 7	Row	6061	6161	*	*	J24
6062 †			5 x 7	Column	6062	6162	*	*	
6072			7 x 9	Row	6072	6172	*	*	
6290	128	Custom	7 x 9	Row	6290	6291	5290	5291	J24
6292			9 x 9	Row/Column	6292	6293	5292	5293	

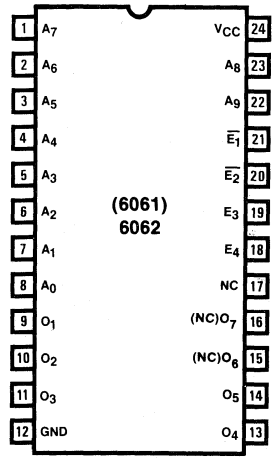
* For military versions of these Character Generators contact the factory.

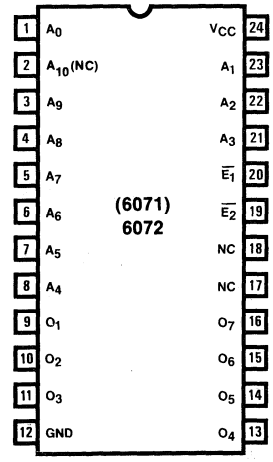
† "OR" enable = $\overline{E1}$ $\overline{E2}$ + E3 E4

Pin Configurations









5

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

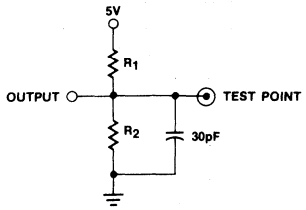
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V				40	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OL} = 8mA	'55, '56, '61, '62			0.5	V
			COM I_{OL} = 10mA					
			I_{OL} = 6mA	'71, '72				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = −1mA		2.4			V
			COM I_{OH} = −2mA					
I_{OZL}	Off-state output current	V_{CC} = MAX, V_O = 0.5V	'55, '56, '61, '62				−50	μA
			'71, '72				−100	
I_{OZH}		V_{CC} = MAX, V_O = 2.4V	'55, '56, '61, '62				50	μA
			'71, '72				100	
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V				100	μA
I_{OS}	Output short-circuit current	V_{CC} = 5V	V_O = 0V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs grounded, All outputs open	Open collector				170	mA
			Three state				180	

Switching Characteristics

Over Operating Conditions

DEVICE TYPE	tAA(ns) ADDRESS ACCESS TIME	tEA(ns) ENABLE ACCESS TIME	tER(ns) ENABLE RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	MAX	R1Ω	R2Ω
6X55, 6X56, 6X61, 6X62	100	70	45	560	1100
5055, 5155	175	90	50		
6X71, 6X72	125	75	40	750	1500

Standard Test Load



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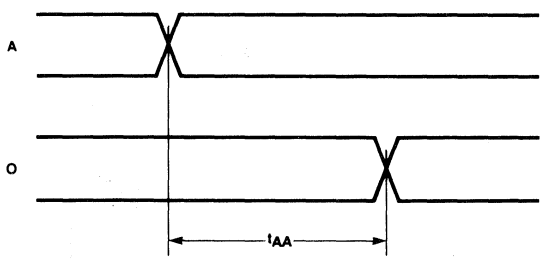
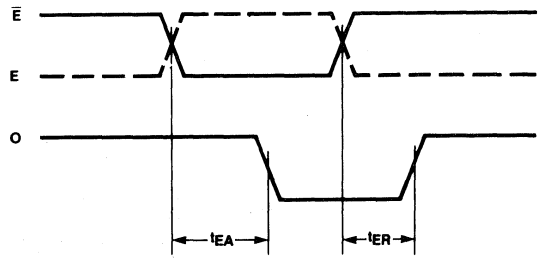
Measurements Made at 1.5V

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

Tabulation by Octal Select-Code

64 ASCII Characters

Row Scan 6055, 6071
Column Scan 6056

	0	1	2	3	4	5	6	7
0	@	A	B	C	D	E	F	G
10	H	I	J	K	L	M	N	O
20	P	Q	R	S	T	U	V	W
30	X	Y	Z	[	\	]	↑	←
40		!	"	#	$	%	&	'
50	(	)	*	+	,	—	.	/
60	0	1	2	3	4	5	6	7
70	8	9	:	;	<	=	>	?

Example:

The Character $ is addressed by the octal code 44

128 ASCII Characters

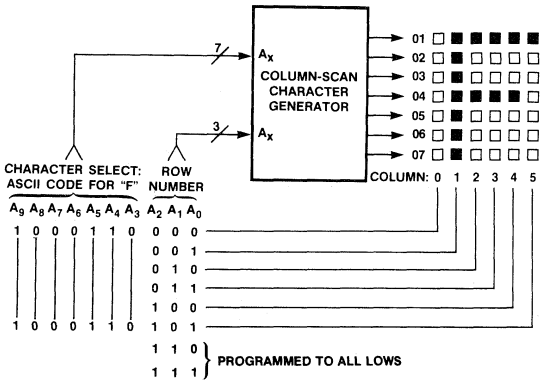
Row Scan 6061, 6072
Column Scan 6062

	0	1	2	3	4	5	6	7
0	△	△	△	△	△	△	△	△
10	△	△	△	△	△	△	△	△
20	△	△	△	△	△	△	△	△
30	△	△	△	△	△	△	△	△
40		!	"	#	$	%	&	'
50	(	)	*	+	,	—	.	/
60	0	1	2	3	4	5	6	7
70	8	9	:	;	<	=	>	?
100	@	A	B	C	D	E	F	G
110	H	I	J	K	L	M	N	O
120	P	Q	R	S	T	U	V	W
130	X	Y	Z	[	\	]	↑	←
140	'	a	b	c	d	e	f	g
150	h	i	j	k	l	m	n	o
160	p	q	r	s	t	u	v	w
170	x	y	z	{	|	}	~	△

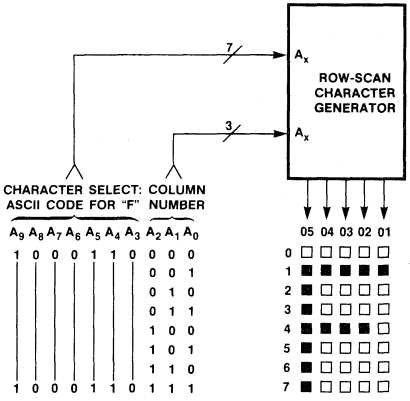
△ This ASCII code represents a control character.
For the corresponding display character see the detailed data sheet.

Generation of the Letter "F"

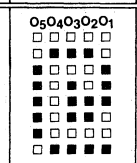
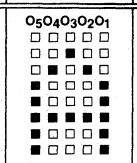
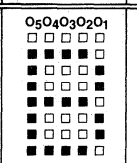
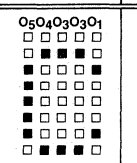
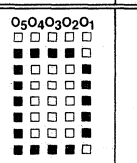
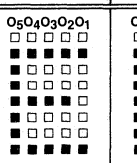
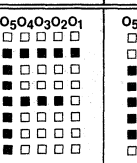
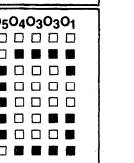
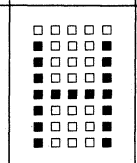
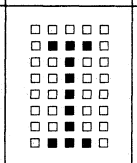
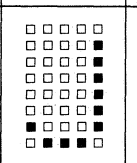
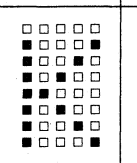
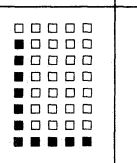
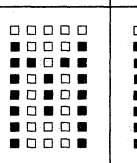
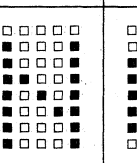
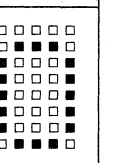
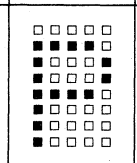
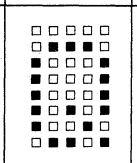
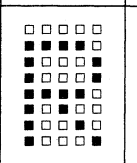
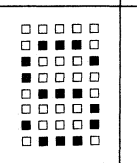
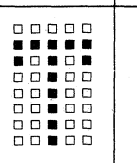
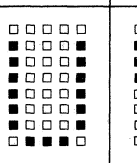
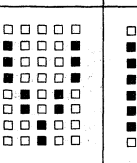
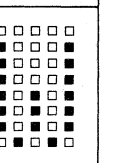
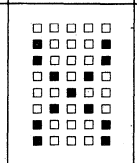
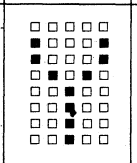
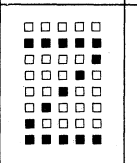
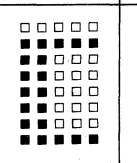
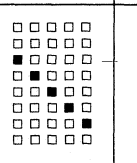
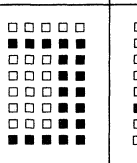
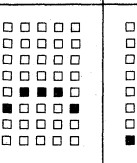
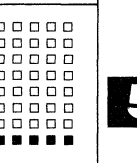
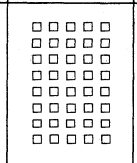
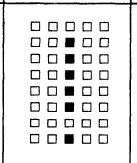
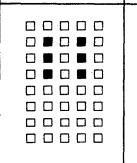
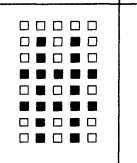
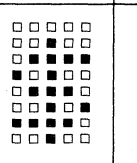
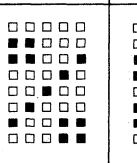
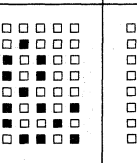
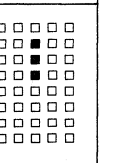
Using Column Scan



Using Row Scan



A "Filled In" Square Represents a Low Memory Output

ASCII INPUT ADDRESS	A_5 A_4 A_3 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
A_8 A_7 A_6 0 0 0								
0 0 1								
0 1 0								
0 1 1								
1 0 0								
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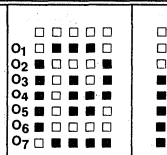
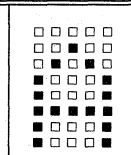
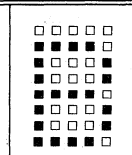
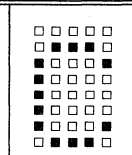
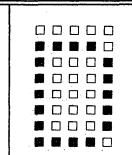
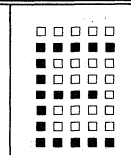
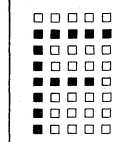
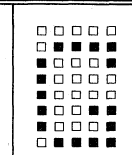
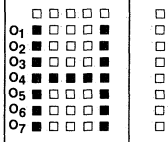
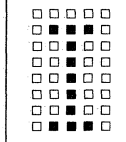
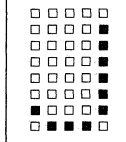
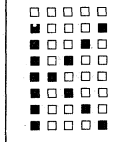
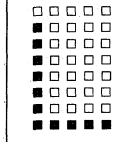
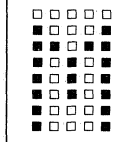
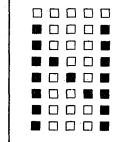
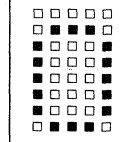
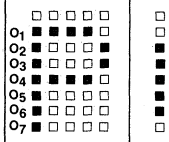
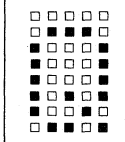
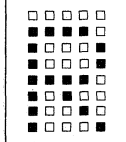
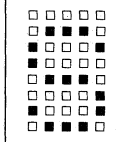
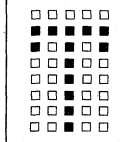
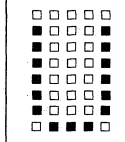
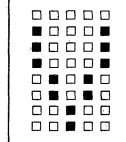
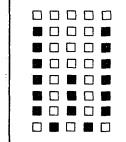
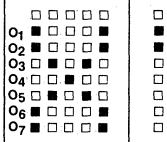
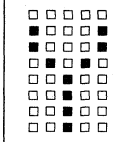
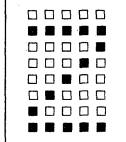
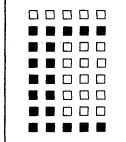
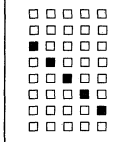
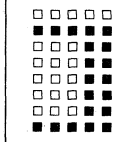
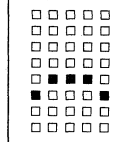
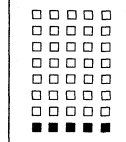
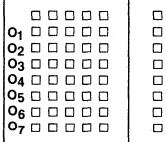
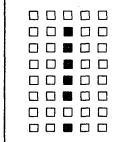
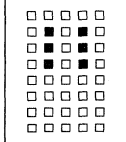
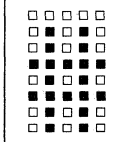
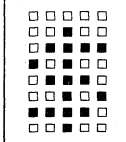
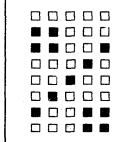
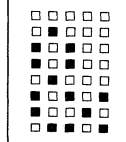
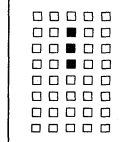
5

A "Filled In" Square Represents a Low Memory Output

ASCII INPUT ADDRESS	A_5 A_4 A_3 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
A_8 A_7 A_6 0 0 0								
0 0 1								
0 1 0								
0 1 1								
1 0 0								
1 0 1								
1 1 0								
1 1 1								

A "Filled In" Square Represents a Low Memory Output

ASCII INPUT ADDRESS	A_6 A_5 A_4 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
A_9 A_8 A_7 0 0 0	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$
0 0 1								
0 1 0								
0 1 1								
1 0 0								
1 0 1								
1 1 0								
1 1 1								

5

A "Filled In" Square Represents a Low Memory Output

ASCII INPUT ADDRESS	A_5 A_4 A_3 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
A_9 A_8 A_7 A_6 0 0 0 0	$O_5O_4O_3O_2O_1$ (NUL)*	$O_5O_4O_3O_2O_1$ (SOH)*	$O_5O_4O_3O_2O_1$	$O_5O_4O_3O_2O_1$ (ETX)*	$O_5O_4O_3O_2O_1$ (EOT)*	$O_5O_4O_3O_2O_1$ (ENQ)*	$O_5O_4O_3O_2O_1$ (ACK)*	$O_5O_4O_3O_2O_1$ (BEL)*
0 0 0 1	(BS)*	(HT)*	(LF)*	(VT)*	(FF)*	(CR)*	(SO)*	(SI)*
0 0 1 0	(DLE)*	(DC1)*	(DC2)*	(DC3)*	(DC4)*	(NAK)*	(SYN)*	(ETB)*
0 0 1 1	(CAN)*	(EM)*	(SUB)*	(ESC)*	(FS)*	(GS)*	(RS)*	(US)*
0 1 0 0								
0 1 0 1								
0 1 1 0								
0 1 1 1								

*The letters in parenthesis identify the control code corresponding to the appropriate pictorial represention. These representations were obtained from the USASI X 3.2 Code Practice Manual.

A "Filled In" Square Represents a Low Memory Output

ASCII INPUT ADDRESS	A_5 A_4 A_3 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
A_9 A_8 A_7 A_6 1 0 0 0	$O_5O_4O_3O_2O_1$	$O_5O_4O_3O_2O_1$	$O_5O_4O_3O_2O_1$	$O_5O_4O_3O_2O_1$	$O_5O_4O_3O_2O_1$	$O_5O_4O_3O_2O_1$	$O_5O_4O_3O_2O_1$	$O_5O_4O_3O_2O_1$
1 0 0 1								
1 0 1 0								
1 0 1 1								
1 1 0 0								
1 1 0 1								
1 1 1 0								
1 1 1 1								(DEL)*

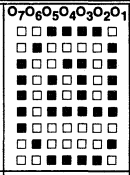
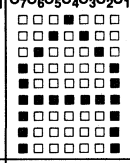
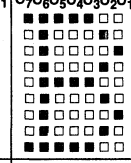
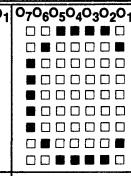
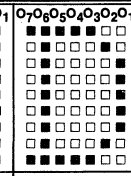
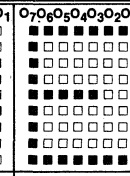
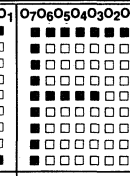
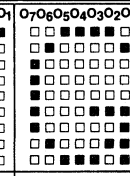
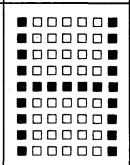
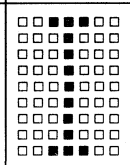
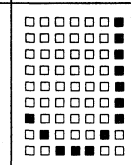
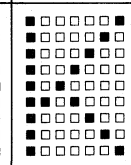
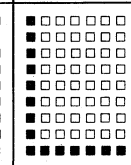
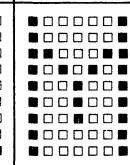
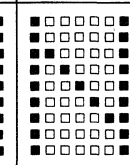
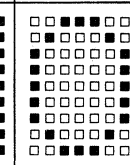
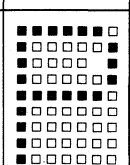
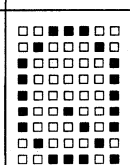
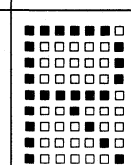
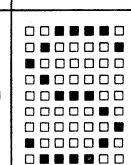
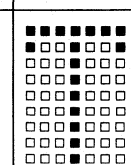
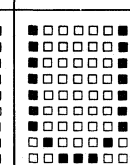
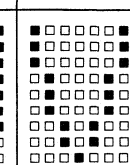
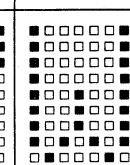
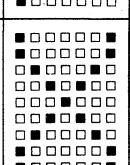
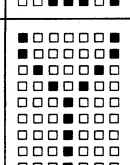
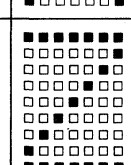
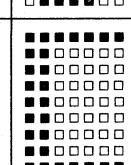
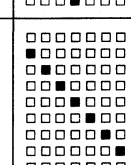
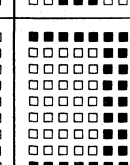
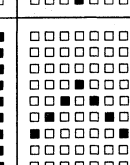
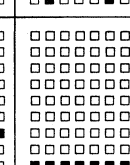
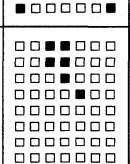
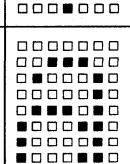
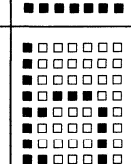
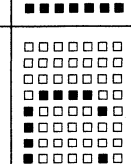
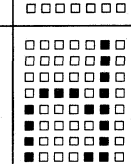
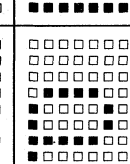
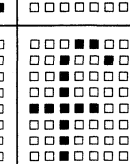
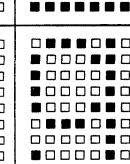
5

A "Filled In" Square Represents a Low Memory Output

ASCII INPUT ADDRESS	A_6 A_5 A_4 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
A_{10} A_9 A_8 A_7 0 0 0 0	$O_7O_6O_5O_4O_3O_2O_1$ (NUL)*	$O_7O_6O_5O_4O_3O_2O_1$ (SOH)*	$O_7O_6O_5O_4O_3O_2O_1$	$O_7O_6O_5O_4O_3O_2O_1$ (ETX)*	$O_7O_6O_5O_4O_3O_2O_1$ (EOT)*	$O_7O_6O_5O_4O_3O_2O_1$ (ENQ)*	$O_7O_6O_5O_4O_3O_2O_1$ (ACK)*	$O_7O_6O_5O_4O_3O_2O_1$ (BEL)*
0 0 0 1	(BS)*	(HT)*	(LF)*	(VT)*	(FF)*	(CR)*	(SO)*	(SI)*
0 0 1 0	(DLE)*	(DC1)*	(DC2)*	(DC3)*	(DC4)*	(NAK)*	(SYN)*	(ETB)*
0 0 1 1	(CAN)*	(EM)*	(SUB)*	(ESC)*	(FS)*	(GS)*	(SX)*	(US)*
0 1 0 0								
0 1 0 1								
0 1 1 0								
0 1 1 1								

*The letters in parenthesis identify the control code corresponding to the appropriate pictorial represention. These representations were obtained from the USASI X 3.2 Code Practice Manual.

A "Filled In" Square Represents a Low Memory Output

ASCII INPUT ADDRESS	A_6 A_5 A_4 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
$A_{10}A_9A_8A_7$ 1 0 0 0								
1 0 0 1								
1 0 1 0								
1 0 1 1								
1 1 0 0								
1 1 0 1								
1 1 1 0								
1 1 1 1								(DEL)*

5

High Speed Custom Character Generators

52/6290 52/6291 52/6292 52/6293

Features/Benefits

- **Schottky—high speed 10MHz**
- **Specifically designed for custom 7 x 9 row scan and 9 x 9 font character generators**
- **Up to 128 characters in one package**
- **Low power dissipation—500mW**
- **Standard packaging—24 pin dip**
- **Single 5 volt supply**
- **125 ns max. access time**

Applications

- **A single package high speed bipolar replacement for slow multiple package MOS character generators**
- **CRT displays**
- **Printing calculators**
- **LED arrays**
- **Typesetting**
- **Navigation systems**

Description

A 7 x 9 font row scan character has 7 outputs and 9 rows per character. The character is formed one row at a time. 9 words of a ROM with 7 outputs per word are required for each character. 128 characters required on 1152 x 7 ROM which is the size of the 5290/1, 6290/1. For custom column scan 7 x 9 characters consult the standard bipolar 7 x 9 character generator data sheet.

A 9 x 9 font character has 9 outputs and 9 rows of columns per character depending upon whether we are forming a row or column scan. 9 words of a ROM with 9 outputs per row are required for each character. 128 characters require an 1152 x 9 ROM which is the 5292/3, 6292/3.

A_3, A_2, A_1, and A_0 pins are used to scan through the 9 ROM words per character. This is usually implemented by "short counting" a 4-bit binary counter so that it counts from 0000 to 1000 (9 counts) continuously (See applications section). A_4 thru A_{10} are used to pick one of the 128 characters. A_4 is the least significant binary digit and A_{10} is the most significant binary digit.

The enable E_1, and E_2 must both be low to activate the part. A disabled part (E_1 or E_2 high) has high memory outputs permitting wire ORing or blanking.

Unused scan locations generate low outputs.

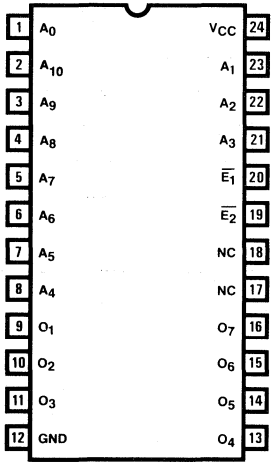
Custom Font

It's easy to go from custom font to the punched card or tape format preferred by Monolithic Memories Inc. Several examples are shown. We have arbitrarily assumed that a character is formed by a series of low memory outputs in a background of high memory outputs. The assumption, of course can be reversed.

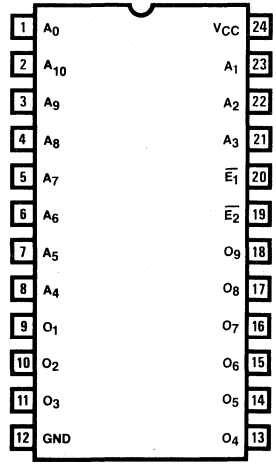
5

Pin Configuration

5290/1, 6290/1 (7 x 9 Row Scan)



5292/3, 6292/3 (9 x 9 Row or Column Scan)



Note 1): A_0, A_1, A_2, A_3 are used for the character scan.
2): Both enables must be low to advance the device.

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

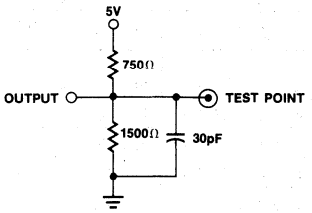
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V			–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			40	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 6mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = –1mA	2.4			V
			COM I_{OH} = –2mA				
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V			–100	μA
I_{OZH}		V_{CC} = MAX	V_O = 2.4V			100	μA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current	V_{CC} = 5V	V_O = 0V	–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded All outputs open	Open collector			170	mA
			Three state			180	

Switching Characteristics

Over Operating Conditions

DEVICE TYPE	tAA(ns) ADDRESS ACCESS TIME	tEA(ns) ENABLE ACCESS TIME	tER(ns) ENABLE RECOVERY TIME
	MAX	MAX	MAX
6290/1, 6292/3	125	75	40
5290/1, 5292/3	150	85	50

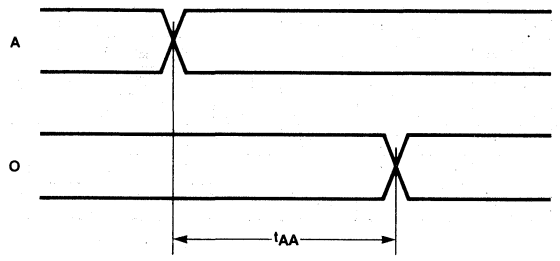
Standard Test Load



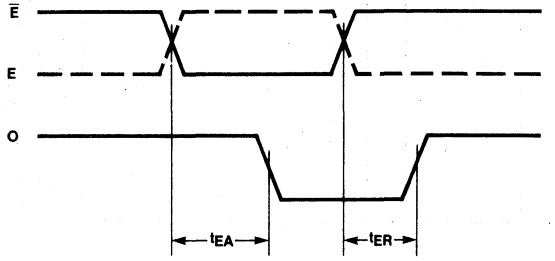
Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V

5

Definition of Waveforms



Address Access Time



Enable Access Time and Recovery Time

Custom Truth Table Coding—5290/1, 6290/1

7 x 9 ROW SCAN

The characters $, &, *, are shown below along with the ROM coding. A "filled in" dot is arbitrarily coded with a low (L)

CHARACTER SELECT								A_3	A_2	A_1	A_0	ROM WORD (DECIMAL)	OUTPUTS							FONT						
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4							O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_7	O_6	O_5	O_4	O_3	O_2	O_1
L	L	L	L	L	L	L	CHARACTER #1	0	0	0	0	0	H	H	L	H	L	H	H	□	□	■	□	■	□	□
								0	0	0	1	1	H	L	L	L	L	L	L	□	■	■	■	■	■	■
								0	0	1	0	2	L	H	L	H	L	H	H	■	□	■	□	■	□	□
								0	0	1	1	3	L	H	L	H	L	H	H	■	□	■	□	■	□	□
								0	1	0	0	4	H	L	L	L	L	L	H	□	■	■	■	■	■	□
								0	1	0	1	5	H	H	L	H	L	H	L	□	□	■	□	■	□	■
								0	1	1	0	6	H	H	L	H	L	H	L	□	□	■	□	■	□	■
								0	1	1	1	7	L	L	L	L	L	L	H	■	■	■	■	■	■	□
								1	0	0	0	8	H	H	L	H	L	H	H	□	□	■	□	■	□	□
L	L	L	L	L	L	H	CHARACTER #2					9	H	L	L	H	H	H	H	□	■	■	□	□	□	□
												10	L	H	H	L	H	H	H	■	□	□	■	□	□	□
												11	L	H	H	L	H	H	H	■	□	□	■	□	□	□
												12	H	L	L	H	H	H	H	□	■	■	□	□	□	□
												13	H	L	L	H	H	H	H	□	■	■	□	□	□	□
												14	L	H	H	L	H	L	H	■	□	□	■	□	■	□
												15	L	H	H	H	L	L	H	■	□	□	□	■	■	□
												16	L	H	H	H	H	L	H	■	□	□	□	□	■	□
												17	H	L	L	L	L	H	L	□	■	■	■	■	□	■
H	H	H	H	H	H	H	CHARACTER #128					1143	H	H	H	L	H	H	H	□	□	□	■	□	□	□
												1144	L	H	H	L	H	H	L	■	□	□	■	□	□	■
												1145	H	L	H	L	H	L	H	□	■	□	■	□	■	□
												1146	H	H	L	L	L	H	H	□	□	■	■	■	□	□
												1147	H	H	H	L	H	H	H	□	□	□	■	□	□	□
												1148	H	H	L	L	L	H	H	□	□	■	■	■	□	□
												1149	H	L	H	L	H	L	H	□	■	□	■	□	■	□
												1150	L	H	H	L	H	H	L	■	□	□	■	□	□	■
												1151	H	H	H	L	H	H	H	□	□	□	■	□	□	□

Use of Custom Truth Table Form—5290/1, 6290/1

Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is shown below coded to the 7 x 9 Row Scan example:

WORD NUMBER	OUTPUTS						
PIN	16	15	14	13	11	10	9
	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0	H	H	L	H	L	H	H
1	H	L	L	L	L	L	L
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1151	H	H	H	L	H	H	H

NOTE:
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 511 = HHHHHHHHH.

Custom Truth Table Coding—5292/3, 6292/3

9 x 9 COLUMN SCAN

The characters $, &, *, can be seen in the font if this page is rotated 90° clockwise. A "filled in" dot is arbitrarily coded with a low (L).

9 x 9 ROW SCAN

The 9 x 9 row scan translation would be similar to the 7 x 9 row scan previously shown except that there would be a 9 x 9 font for each character and outputs 8 and 9 in the ROM would be used and coded.

CHARACTER SELECT								ROM WORD (DECIMAL)	OUTPUTS									FONT								
A_{10}	A_9	A_8	A_7	A_6	A_5	A_4			O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
L	L	L	L	L	L	L	CHARACTER #1	8	H	L	H	H	H	L	L	H	H	□	■	□	□	□	■	■	□	□
								7	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								6	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								5	L	L	L	L	L	L	L	L	L	■	■	■	■	■	■	■	■	■
								4	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								3	L	L	L	L	L	L	L	L	L	■	■	■	■	■	■	■	■	■
								2	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								1	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
								0	H	H	L	L	H	H	H	L	H	□	□	■	■	□	□	□	■	□
L	L	L	L	L	L	H	CHARACTER #2	17	H	H	H	H	H	H	H	H	H	□	□	□	□	□	□	□	□	□
								16	H	H	H	H	H	H	L	H	L	□	□	□	□	□	□	■	□	■
								15	H	H	H	H	H	H	L	L	H	□	□	□	□	□	□	■	■	□
								14	H	H	H	H	H	H	L	H	L	□	□	□	□	□	□	■	□	■
								13	H	L	L	L	L	L	H	H	L	□	■	■	■	■	■	□	□	■
								12	L	H	H	L	L	H	H	H	L	■	□	□	■	■	□	□	□	■
								11	L	H	H	L	L	H	H	H	L	■	□	□	■	■	□	□	□	■
								10	L	H	H	L	L	H	H	L	H	■	□	□	■	■	□	□	■	□
								9	H	L	L	H	H	L	L	H	H	□	■	■	□	□	■	■	□	□
≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈	≈
H	H	H	H	H	H	H	CHARACTER #128	1151	H	H	H	H	H	H	H	H	H	□	□	□	□	□	□	□	□	□
								1150	H	L	H	H	H	H	H	L	H	□	■	□	□	□	□	□	■	□
								1149	H	H	L	H	H	H	L	H	H	□	□	■	□	□	□	■	□	□
								1148	H	H	H	L	H	L	H	H	H	□	□	□	■	□	■	□	□	□
								1147	L	L	L	L	L	L	L	L	L	■	■	■	■	■	■	■	■	■
								1146	H	H	H	L	H	L	H	H	H	□	□	□	■	□	■	□	□	□
								1145	H	H	L	H	H	H	L	H	H	□	□	■	□	□	□	■	□	□
								1144	H	L	H	H	H	H	H	L	H	□	■	□	□	□	□	□	■	□
								1143	H	H	H	H	H	H	H	H	H	□	□	□	□	□	□	□	□	□

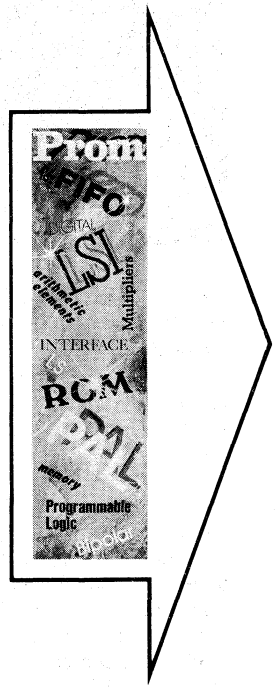
Use of Custom Truth Table Form—5292/3, 6292/3

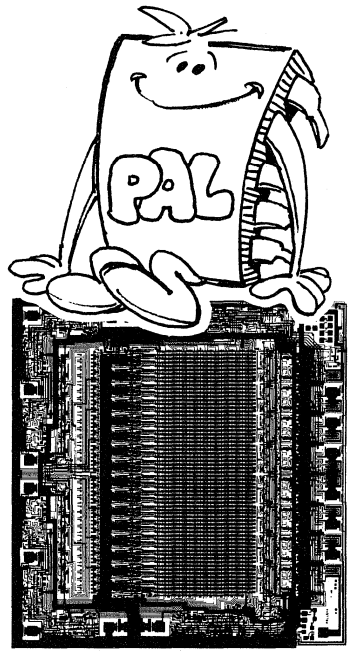
Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is shown below coded to the 9 x 9 column scan example:

WORD NUMBER	OUTPUTS								
PIN	18	17	16	15	14	13	11	10	9
	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0	H	H	L	L	H	H	H	L	H
1	H	L	H	H	L	H	H	L	H
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1151	H	H	H	H	H	H	H	H	H

NOTE:
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 511 = HHHHHHHHH.

5





The PAL™ Concept

Monolithic Memories' family of PAL devices gives designers a powerful tool with unique capabilities for use in new and existing logic designs. The PAL saves time and money by solving many of the system partitioning and interface problems brought about by increases in semiconductor device technology.

Rapid advances in large scale integration technology have led to larger and larger standard logic functions; single I.C.s now perform functions that formerly required complete circuit cards. While LSI offers many advantages, advances have been made at the expense of device flexibility. Most LSI devices still require large numbers of SSI/MSI devices for interfacing with user systems. Designers are still forced to turn to random logic for many applications.

The "complexity gap" between TTL and LSI devices has led to ineffective use of both. The TTL provides the speed and flexibility, but it is ineffective in terms of package count, power consumption, and P.C. board space. LSI offers high functional density and low power consumption, but it is slow and rigidly partitioned. Even the microprocessor, widely acclaimed for its flexibility, is slow and expensive when the costs of programming and support interfaces are considered.

The designer is confronted with another problem when a low to medium complexity product is designed. Often the function is well defined and could derive significant benefits from fabrication as an integrated circuit. However, the design cycle for a custom circuit is long and the costs can be very high. This makes the risk significant enough to deter most users. The technology to support maximum flexibility combined with fast turn around on custom logic has simply not been available.

Attempts to solve these problems have led to increasing interest in fuse programmable logic devices. These devices can all be user configured to provide custom functions. PROMs, FPLAs, FPGAs, and PMUXs have all been used in this way. These approaches have met with some success, but all are deficient in one or more areas. PROMs require careful design to avoid undesirable data transitions; FPLAs are expensive, difficult to program and complex to understand; FPGAs and PMUXs are not widely available and lack flexibility. All of these devices still require extensive interface logic for use in systems.

The PAL family offers a fresh approach to using fuse programmable logic. PALs are a conceptually unified group of devices which combine programmable flexibility with high speed and an extensive selection of interface options. PALs can lower inventory, cut design cycles and provide high complexity with maximum flexibility. These features, combined with lower package count and high reliability, truly make the PAL a circuit designer's best friend.

The PAL—Teaching Old PROMs New Tricks

MMI developed the modern PROM and introduced many of the architectures and techniques now regarded as industry standards. As the world's largest PROM manufacturer, MMI has the proven technology and high volume production capability required to manufacture and support the PAL.

The PAL is an extension of the fusible link technology pioneered by Monolithic Memories for use in bi-polar PROMs. The fusible link PROM first gave the digital systems designer the power to "write on silicon." In a few seconds he was able to transform a blank PROM from a general purpose device into one containing a custom algorithm, microprogram, or Boolean transfer function. This opened up new horizons for the use of PROMs in computer control stores, character generators, data storage tables and many other applications. The wide acceptance of this technology is clearly demonstrated by today's multi-million dollar PROM market.

The key to the PROM's success is that it allows the designer to quickly and easily customize the chip to fit his unique requirements. The PAL extends this programmable flexibility by utilizing proven fusible link technology to implement logic functions. Using PALs the designer can quickly and effectively implement custom logic varying in complexity from random gates to complex arithmetic functions.

ANDs and ORs

The PAL implements the familiar sum of products logic by using a programmable AND array whose output terms feed a fixed OR array. Since the sum of products form can express any Boolean transfer function, the PAL's uses are only limited by the number of terms available in the AND - OR arrays. PAL's come in different sizes to allow for effective logic optimization.

Figure 1 shows the basic PAL structure for a two input, one output logic segment. The general logic equation for this segment is

$$\text{Output} = (I_1+\overline{f_1})(\overline{I_1}+\overline{f_2})(I_2+\overline{f_3})(\overline{I_2}+\overline{f_4}) +$$
$$(I_1+\overline{f_5})(\overline{I_1}+\overline{f_6})(I_2+\overline{f_7})\ (\overline{I_2}+\overline{f_8})$$

where the "f" terms represent the state of the fusible links in the PAL's AND array. An unblown link represents a logic 1. Thus,

fuse blown, f = 0

fuse intact, f = 1

An unprogrammed PAL has all fuses intact.

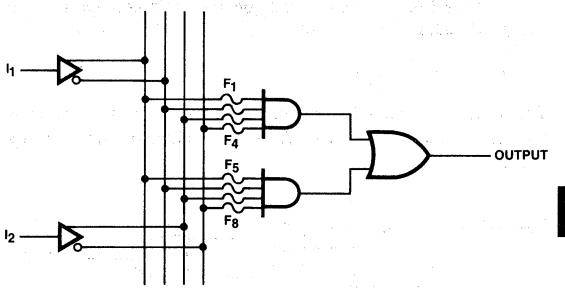


Figure 1

New Device, New Notation

Logic equations, while convenient for small functions, rapidly become cumbersome in large systems. To reduce possible confusion, complex logic networks are generally defined by logic diagrams and truth tables. Figure 2 shows the logic convention adopted to keep PAL logic easy to understand and use. In the figure, an "x" represents an intact fuse used to perform the logic AND function. (Note: the input terms on the common line with the x's are not connected together.) The logic symbology shown in Figure 2 has been informally adopted by integrated circuit manufacturers because it clearly establishes a one-to-one correspondence between the chip layout and the logic diagram. It also allows the logic diagram and truth table to be combined into a compact and easy to read form, thereby serving as a convenient shorthand for PALs. The two input - one output example from Figure 1 redrawn using the new logic convention is shown in Figure 3.

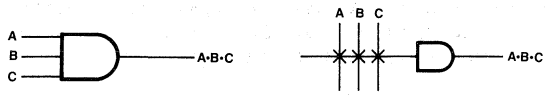


Figure 2

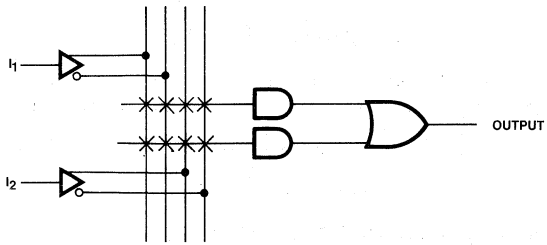


Figure 3

As a simple PAL example, consider the implementation of the transfer function:

$$\text{Output} = I_1\overline{I_2} + \overline{I_1}I_2$$

The normal combinatorial logic diagram for this function is shown in figure 4, with the PAL logic equivalent shown in figure 5.

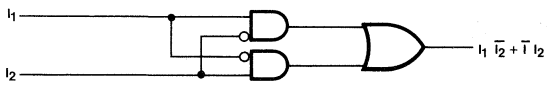


Figure 4

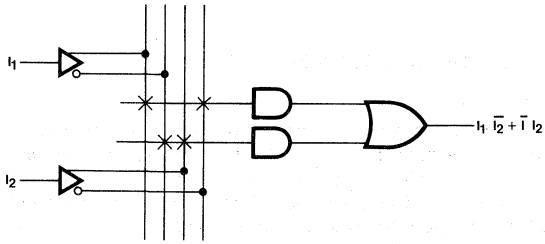


Figure 5

Using this logic convention it is now possible to compare the PAL structure to the structure of the more familiar PROM and PLA. The basic logic structure of a PROM consists of a fixed AND array whose outputs feed a programmable OR array (figure 6). PROMs are low-cost, easy to program, and available in a variety of sizes and organizations. They are most commonly used to store computer programs and data. In these applications the fixed input is a computer memory address; the output is the contents of that memory location.

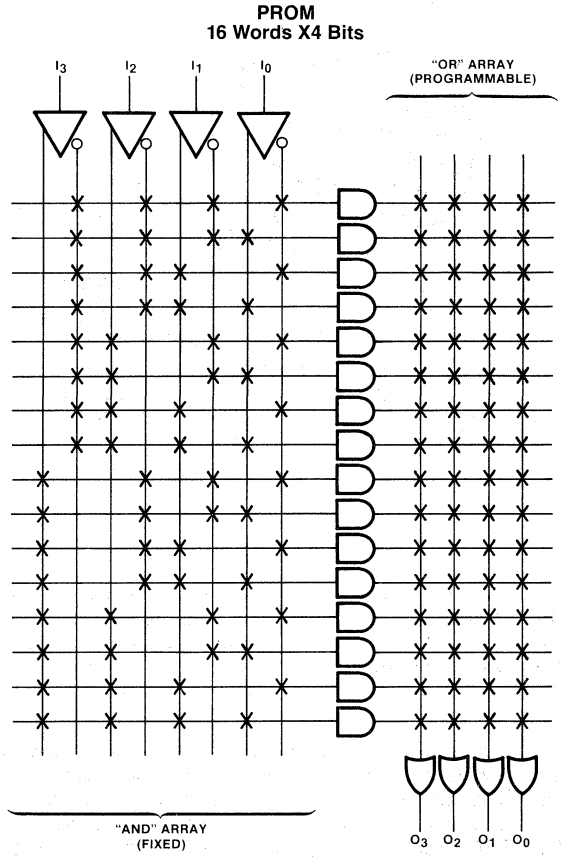


Figure 6

The basic logic structure of the PLA consists of a programmable AND array whose outputs feed a programmable OR array (Figure 7). Since the designer has complete control over all inputs and outputs, the PLA provides the ultimate flexibility for implementing logic functions. They are used in a wide variety of applications. However, this generality makes PLA's expensive, quite formidable to understand, and are costly to program (they require special programmers).

The basic logic structure of the PAL, as mentioned earlier, consists of a programmable AND array whose outputs feed a fixed OR array (Figure 8). The PAL combines much of the flexibility of the PLA with the low cost and easy programmability of the PROM. Table 1 summarizes the characteristics of the PROM, PLA, and PAL logic families.

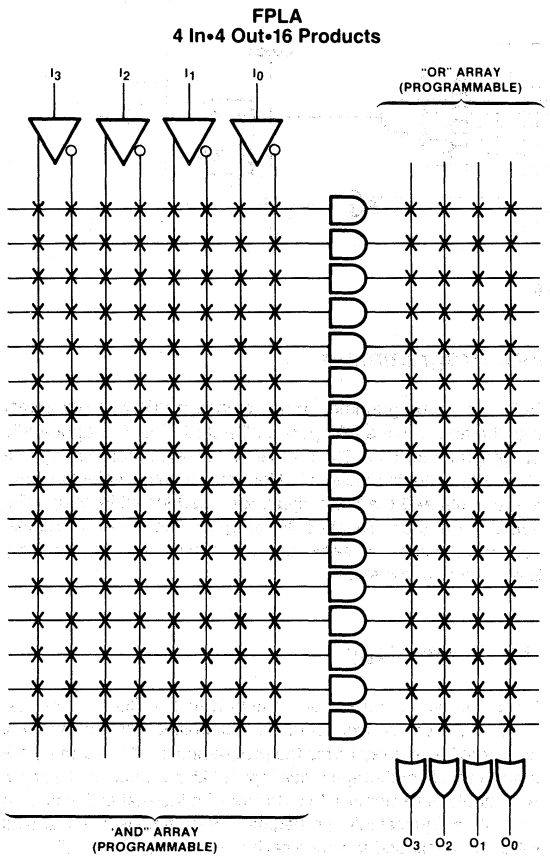


Figure 7

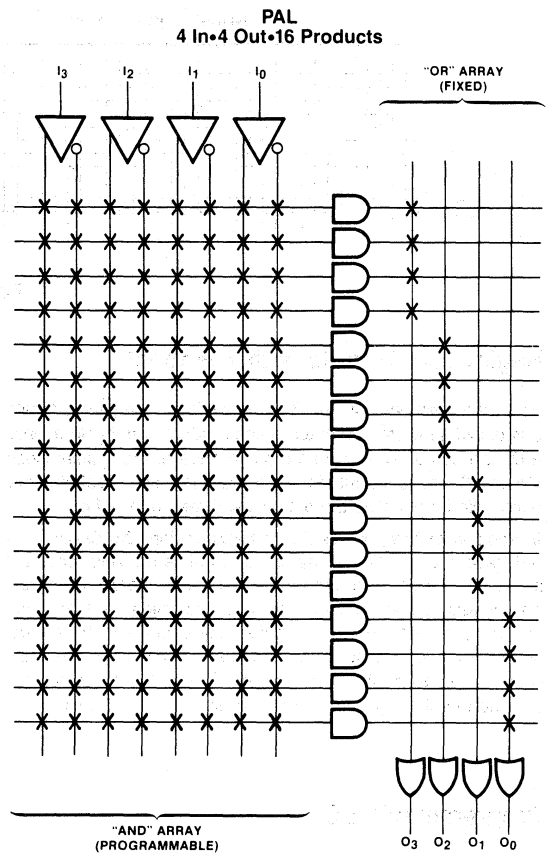


Figure 8

	AND	OR	OUTPUT OPTIONS
PROM	Fixed	Prog	TS, OC
FPLA	Prog	Prog	TS, OC, Fusible Polarity
FPGA	Prog	None	TS, OC, Fusible Polarity
PMUX	Fix/Prog	Fixed	TS
PAL	Prog	Fixed	TS, Registered, Feedback, I/O

Table 1

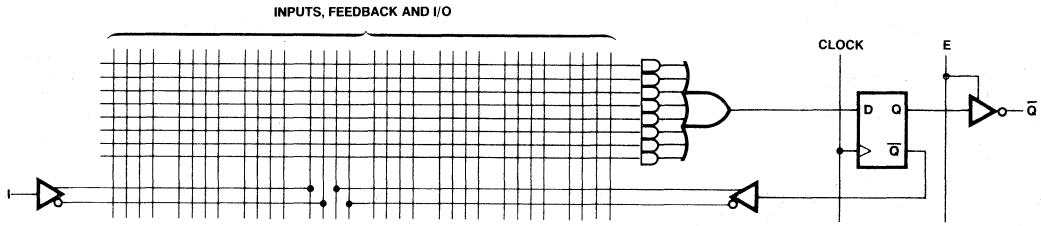


Figure 9

Registered Outputs with Feedback

High end members of the PAL family feature registered data outputs with register feedback. Each product term is stored into a D-type output flip-flop on the rising edge of the system clock (Figure 9). The Q output of the flip-flop can then be gated to the output pin by enabling the active low three-state buffer.

In addition to being available for transmission, the Q output is fed back into the PAL array as an input term. This feedback allows the PAL to "remember" the previous state, and it can alter its function based upon that state. This allows the designer to configure the PAL as a state sequencer which can be programmed to execute such elementary functions as count up, count down, skip, shift, and branch. These functions can be executed by the registered PAL at rates of up to 20 MHz.

Programmable I/O

Another feature of the high-end members of the PAL family is programmable input/output. This allows the product terms to directly control the outputs of the PAL (Figure 10). One product term is used to enable the three-state buffer, which in turn gates the summation term to the output pin. The output is also fed back into the PAL array as an input. Thus the PAL drives the I/O pin when the three-state gate is enabled; the I/O pin is an input to the PAL array when the three-state gate is disabled. This feature can be used to allocate available pins for I/O functions or to provide bi-directional output pins for operations such as shifting and rotating serial data.

PAL Programming

PALs can be programmed in any standard PROM programmer with the addition of a PAL personality card. The PAL appears to the programmer as a 512 x 4 PROM. During programming four of the PAL outputs are selected for programming while the other four outputs and the eight inputs are used for addressing. The outputs are then switched to program the other locations. Verification uses the same procedure with the programming lines held in a low state.

PAL Technology

PALS are manufactured using the proven TTL Schottky bipolar Ti-W fuse process used to make fusible-link PROMs. An NPN emitter follower array forms the programmable AND array. PNP inputs provide high-impedance inputs (.25 mA max.) to the array. All outputs are standard TTL drivers with internal active pull-up transistors. Typical PAL propagation delay time is 25 ns, and all PALs are packaged in space saving 20-pin "skinny-dips".

PAL Data Security

The circuitry used for programming and logic verification can be used at any time to determine the logic pattern stored in the PAL array. For security, the PAL has a "last fuse" which can be blown to disable the verification logic. This provides a significant deterrent to potential copiers, and it can be used to effectively protect proprietary designs.

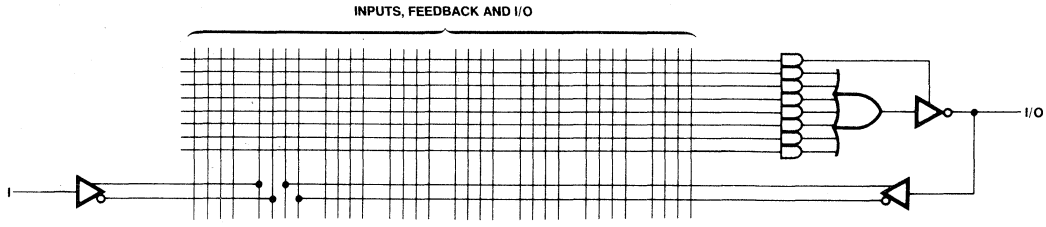
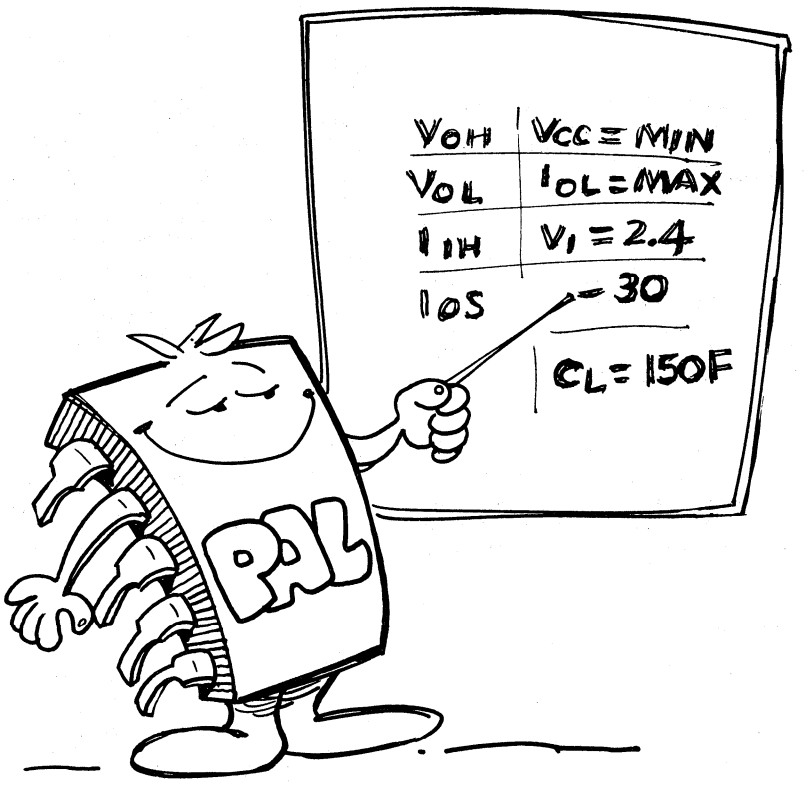


Figure 10

PAL Series 20
Data Sheet



Programmable Array Logic Family

PAL™ Series 20 Data Sheet

U.S. Patent 4124899

Features/Benefits

- **Programmable replacement for conventional TTL logic.**
- **Reduces IC inventories substantially and simplifies their control.**
- **Reduces chip count by 4 to 1.**
- **Expedites and simplifies prototyping and board layout.**
- **Saves space with 20-pin Skinny DIP packages.**
- **High speed: 25ns typical propagation delay.**
- **Programmed on standard PROM programmers.**
- **Programmable three-state outputs.**
- **Special feature reduces possibility of copying by competitors.**

Description

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

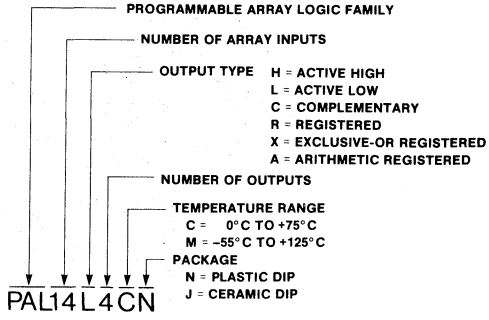
- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback
- Arithmetic capability

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

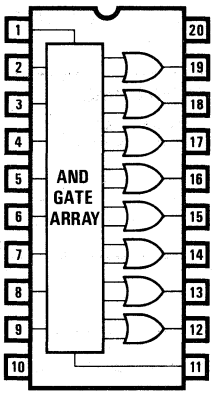
PART NUMBER	DESCRIPTION
PAL10H8	OCTAL 10 INPUT AND-OR GATE ARRAY
PAL12H6	HEX 12 INPUT AND-OR GATE ARRAY
PAL14H4	QUAD 14 INPUT AND-OR GATE ARRAY
PAL16H2	DUAL 16 INPUT AND-OR GATE ARRAY
PAL16C1	16 INPUT AND-OR/AND-OR-INVERT GATE ARRAY
PAL10L8	OCTAL 10 INPUT AND-OR-INVERT GATE ARRAY
PAL12L6	HEX 12 INPUT AND-OR-INVERT GATE ARRAY
PAL14L4	QUAD 14 INPUT AND-OR-INVERT GATE ARRAY
PAL16L2	DUAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL16L8	OCTAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL16R8	OCTAL 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL16R6	HEX 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL16R4	QUAD 16 INPUT REGISTERED AND-OR GATE ARRAY

Ordering Information

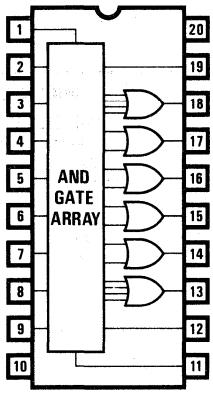


PAL Logic Symbols

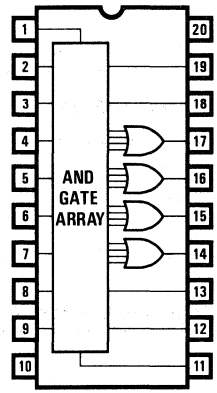
PAL10H8



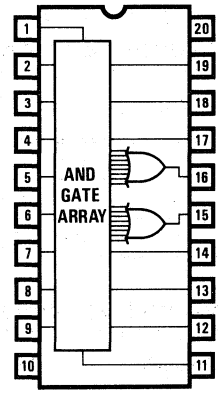
PAL12H6



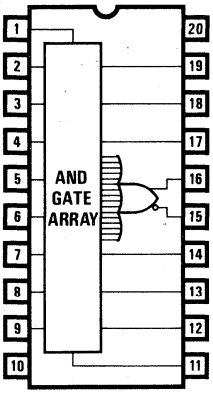
PAL14H4



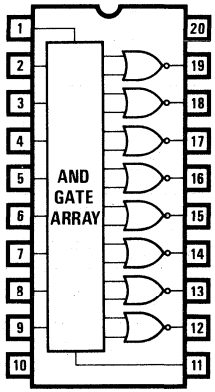
PAL16H2



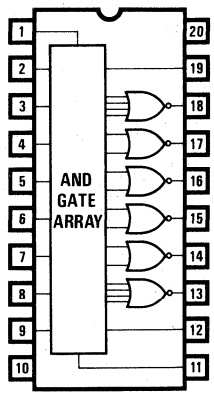
PAL16C1



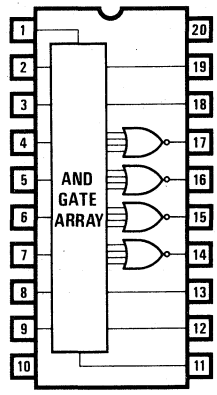
PAL10L8



PAL12L6



PAL14L4



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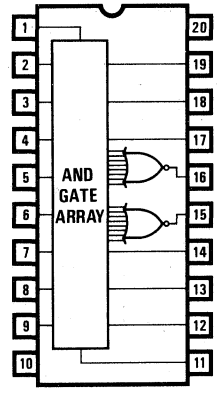

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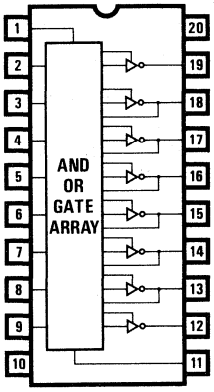

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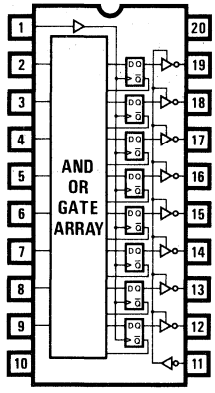

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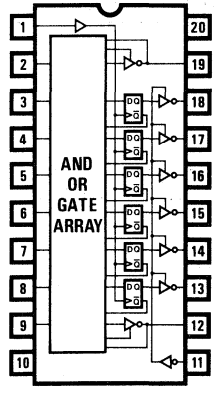

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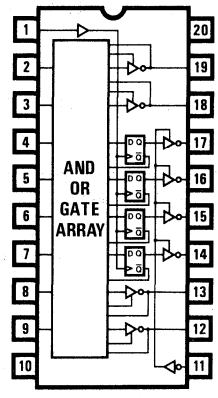


Absolute Maximum Ratings

	Operating	Programming
Supply Voltage, V_{CC}	7	12V
Input Voltage	5.5V	12V*
Off-state output Voltage	5.5V	12V
Storage temperature	−65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature				0		75	°C
T_C	Operating case temperature	−55		125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V				−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	10H8, 12H6, 14H4, 16H2, 16C1, 10L8, 12L6, 14L4, 16L2	MIL / COM I_{OL} = 8mA			0.5	V
			16L8 16R4	MIL I_{OL} = 12mA				
			16R6 16R8	COM I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = −2mA	2.4			V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	Three-state only	V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX	10H8, 12H6, 14H4, 16H2, 16C1, 10L8, 12L6, 14L4, 16L2			55	90	mA
			16L8			140	210	
			16R4, 16R6, 16R8			150	225	

† I/O pin leakage is the worst case of I_{OZX} or I_{IX} e.g., I_{IL} and I_{OZH}

* Pins 1 and 11 may be raised to 22V max.

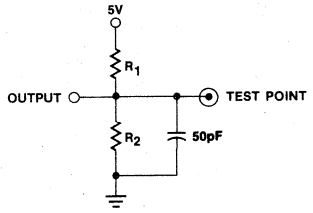
** Only one output shorted at a time.

Switching Characteristics

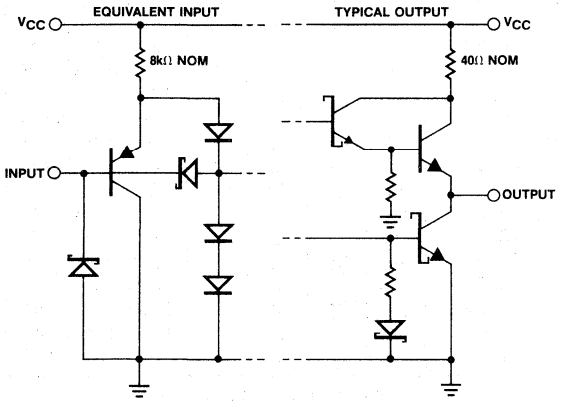
Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input to output		10H8 12H6 14H4 16H2 16C1 10L8 12L6 14L4 16L2 R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	40	ns
t_{PD}	Input or feedback to output		16R8 16R6 16R4 16L8 R_1 = 200Ω R_2 = 390Ω		25	45		25	40	ns
t_{CLK}	Clock to output or feedback				15	25		15	25	ns
t_{PZX}	Pin 11 to output enable				15	25		15	25	ns
t_{PXZ}	Pin 11 to output disable				15	25		15	25	ns
t_{PZX}	Input to output enable				25	45		25	40	ns
t_{PXZ}	Input to output disable				25	45		25	40	ns
t_W	Width of clock	Low		25			25			ns
		High		25			25			
t_{SU}	Setup time from input or feedback	16R8 16R6 16R4		45			40			ns
t_H	Hold time			0	−15		0	−15		ns
f_{MAX}	Maximum frequency	16R8 16R6 16R4		14			16			MHz

Test Load



Schematic of Inputs and Outputs



Approved Programmers

MANUFACTURER	PERSONALITY CARD SET	SOCKET ADAPTER CONFIGURATION
Cybernetic Programming Systems, Inc.	CYMPC-1	
Data I/O Corporation	909-1427	715 1428-1 715 1428-2 715 1428-3
Pro-Log Corporation	PM9068	
Stag Systems	PM202	AM10H8 AM10L8 AM12H6 AM12L6 AM14H4 AM14L4 AM16H2 AM16L2 AM16C1
Structured Design	SD-20	

6

Programming

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all 15 PAL types. The array is divided into two groups, products 0 thru 31 and products 32 thru 63, for which pin identifications are shown in Pin Configurations below. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

Step 1 Raise Output Disable, OD, to V_{IHH}

Step 2 Select an input line by specifying I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7 and L/R as shown in Table 1.

Step 3 Select a product line by specifying A_0, A_1 and A_2 one-of-eight select as shown in Table 2.

Step 4 Raise V_{CC} (pin 20) to V_{IHH}

Step 5 Program the fuse by pulsing the output pins, O, of the selected product group to V_{IHH} as shown in Programming Waveform.

Step 6 Lower V_{CC} (pin 20) to 6.0 V

Step 7 Pulse the CLOCK pin and verify the output pin, O, to be Low for active Low PAL types or High for active High PAL types.

Step 8 Lower V_{CC} (pin 20) to 4.5 V and repeat step 7.

Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see Programming Waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to V_P. V_{CC} is not required during this operation.

Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g., 10kΩ to 5.0V)

INPUT LINE NUMBER	PIN IDENTIFICATION								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

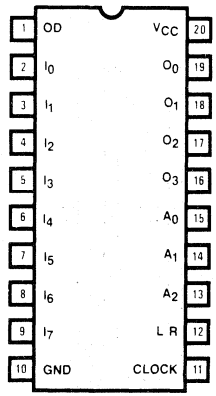
Table 1 Input Line Select

PRODUCT LINE NUMBER	PIN IDENTIFICATION						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

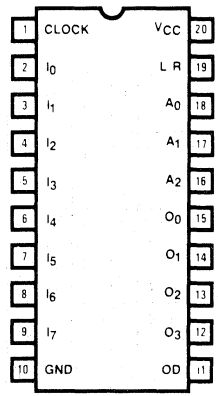
Table 2 Product Line Select

Pin Configurations

PRODUCTS 0 THRU 31



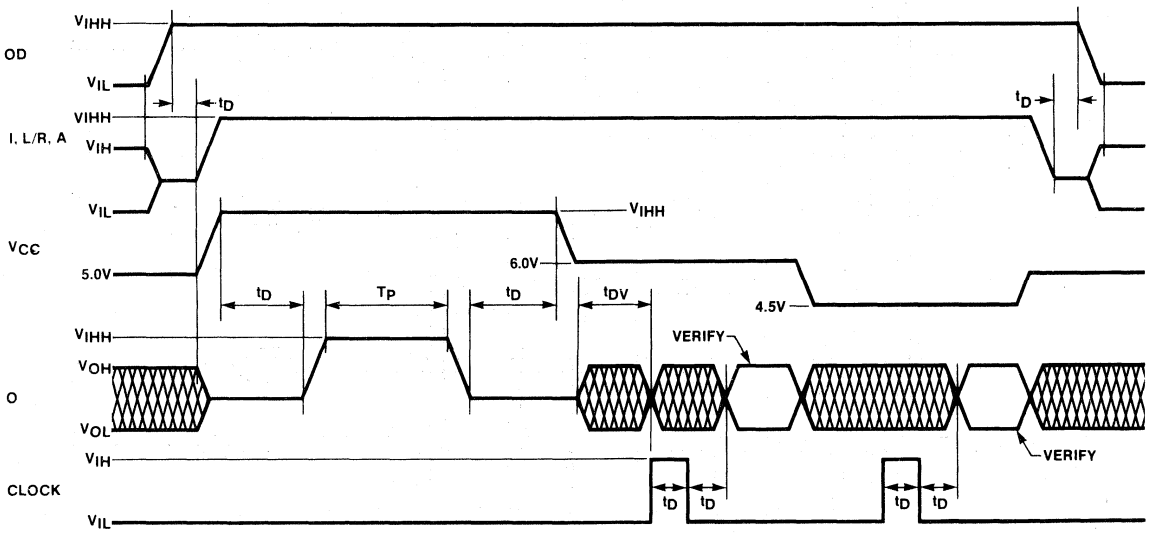
PRODUCTS 32 THRU 63



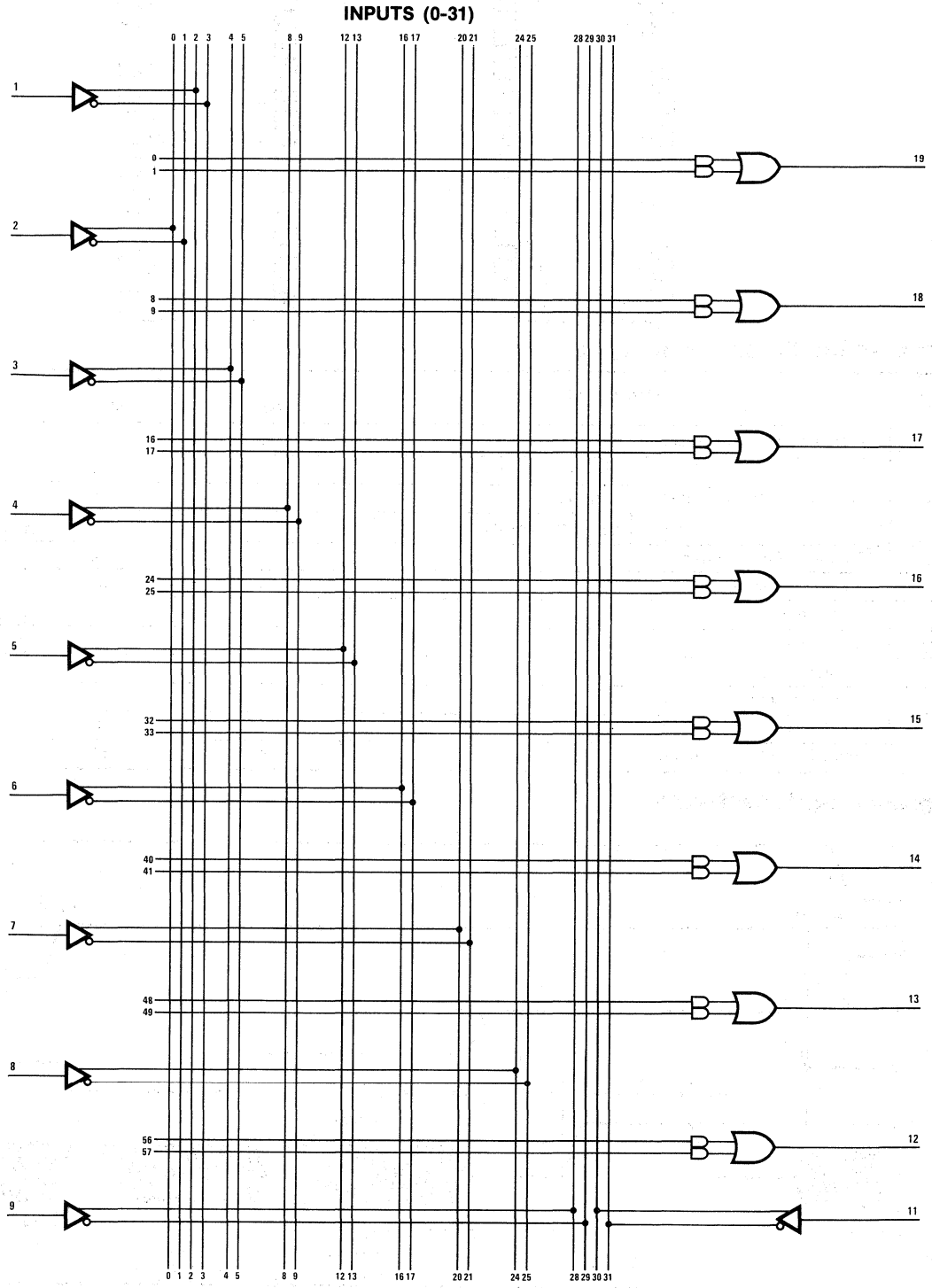
Programming Parameters T_A = 25°C

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNIT
V_{IHH}	Program-level input voltage		11	11.5	12	V
I_{IHH}	Program-level input current	Output Program Pulse			50	mA
		OD, L/R			25	
		All Other Inputs			5	
I_{CCH}	Program Supply Current				400	mA
T_P	Program Pulse Width		10		50	μs
t_D	Delay time		100			ns
t_{DV}	Delay Time to Verify		100			μs
	Program Pulse duty cycle				25	%
V_P	Verify-Protect-input voltage		20	21	22	V
I_P	Verify-Protect-input current				400	mA
T_{PP}	Verify-Protect Pulse Width		20		50	msec

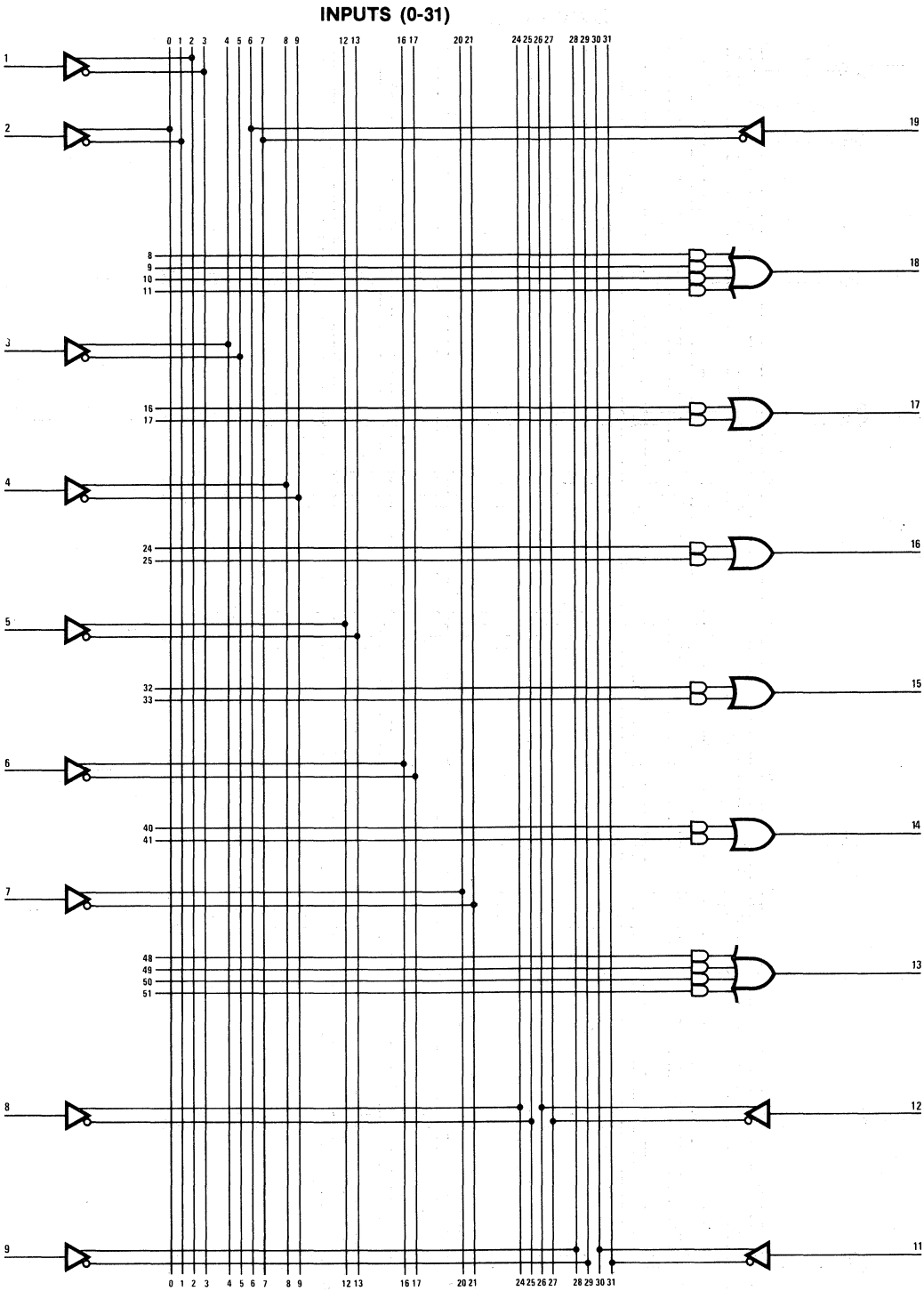
Programming Waveforms



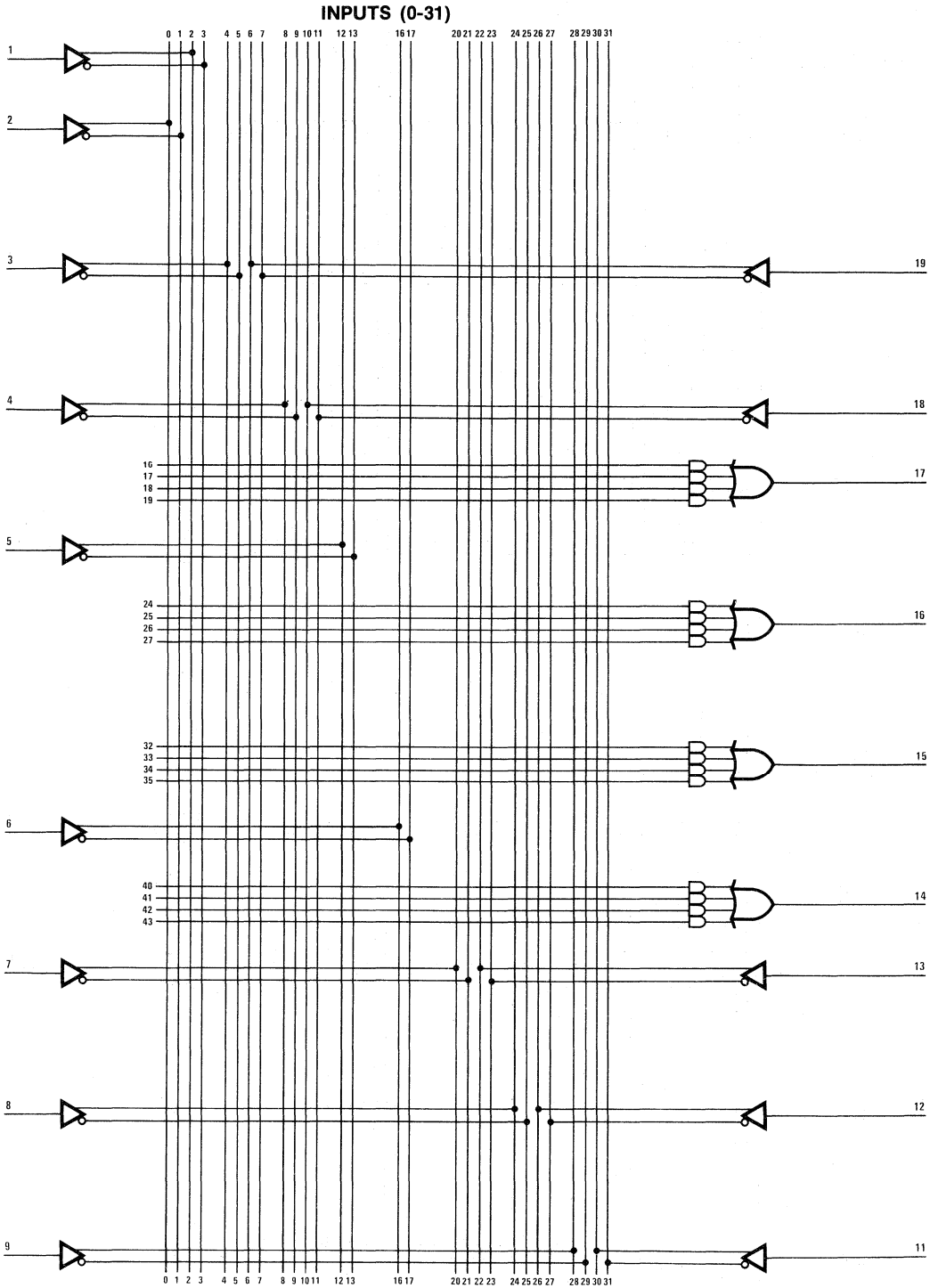
Logic Diagram PAL10H8



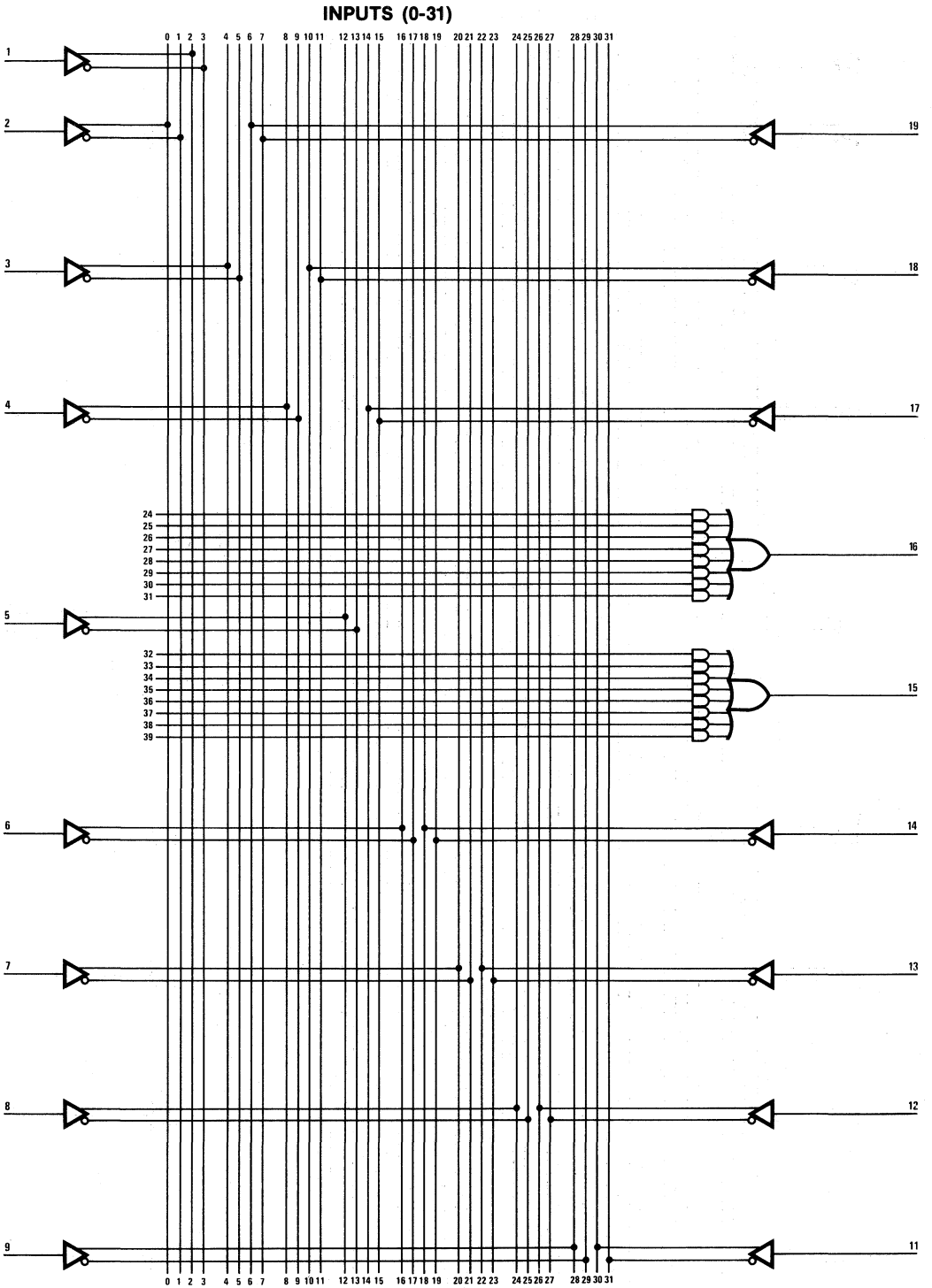
Logic Diagram PAL12H6



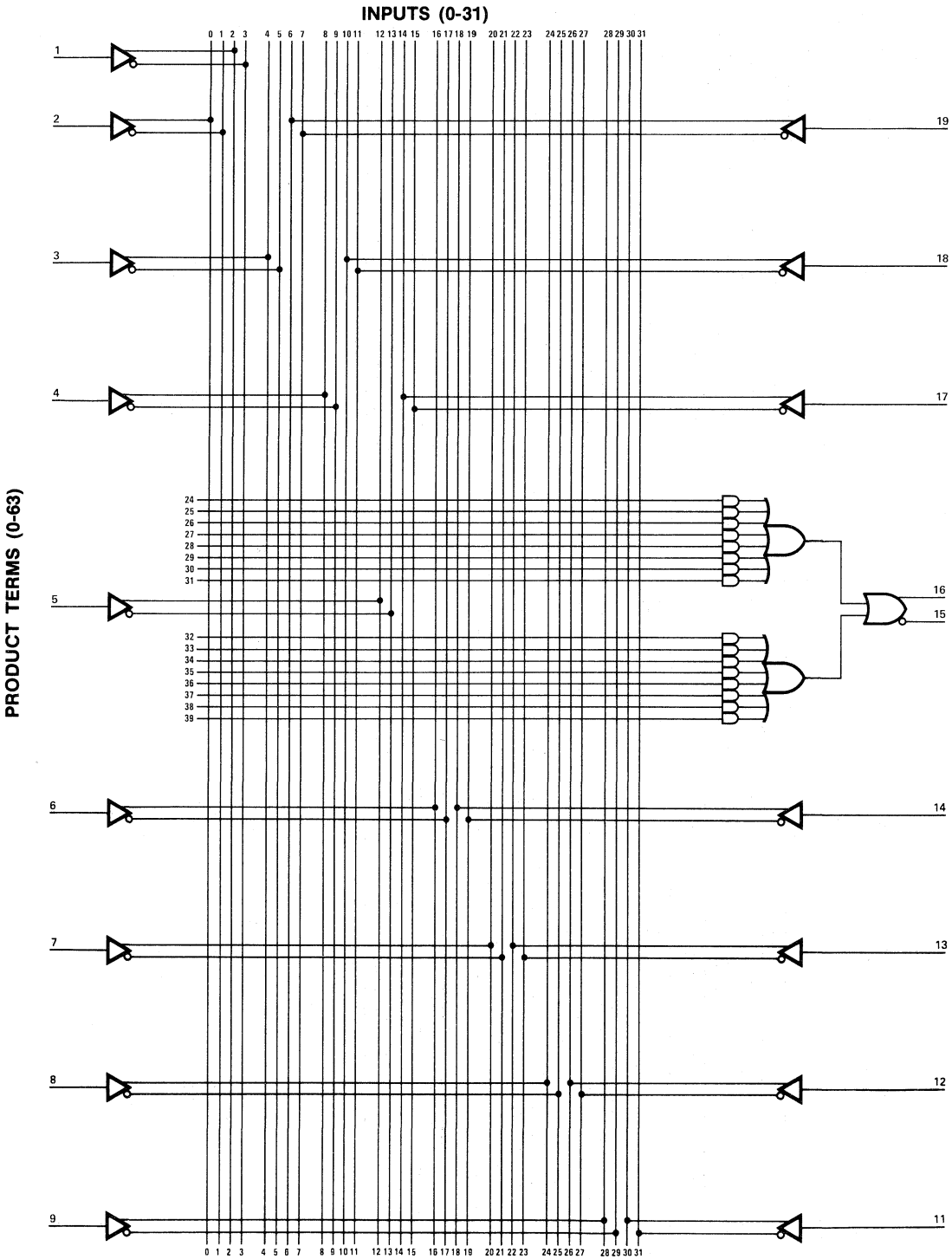
Logic Diagram PAL14H4



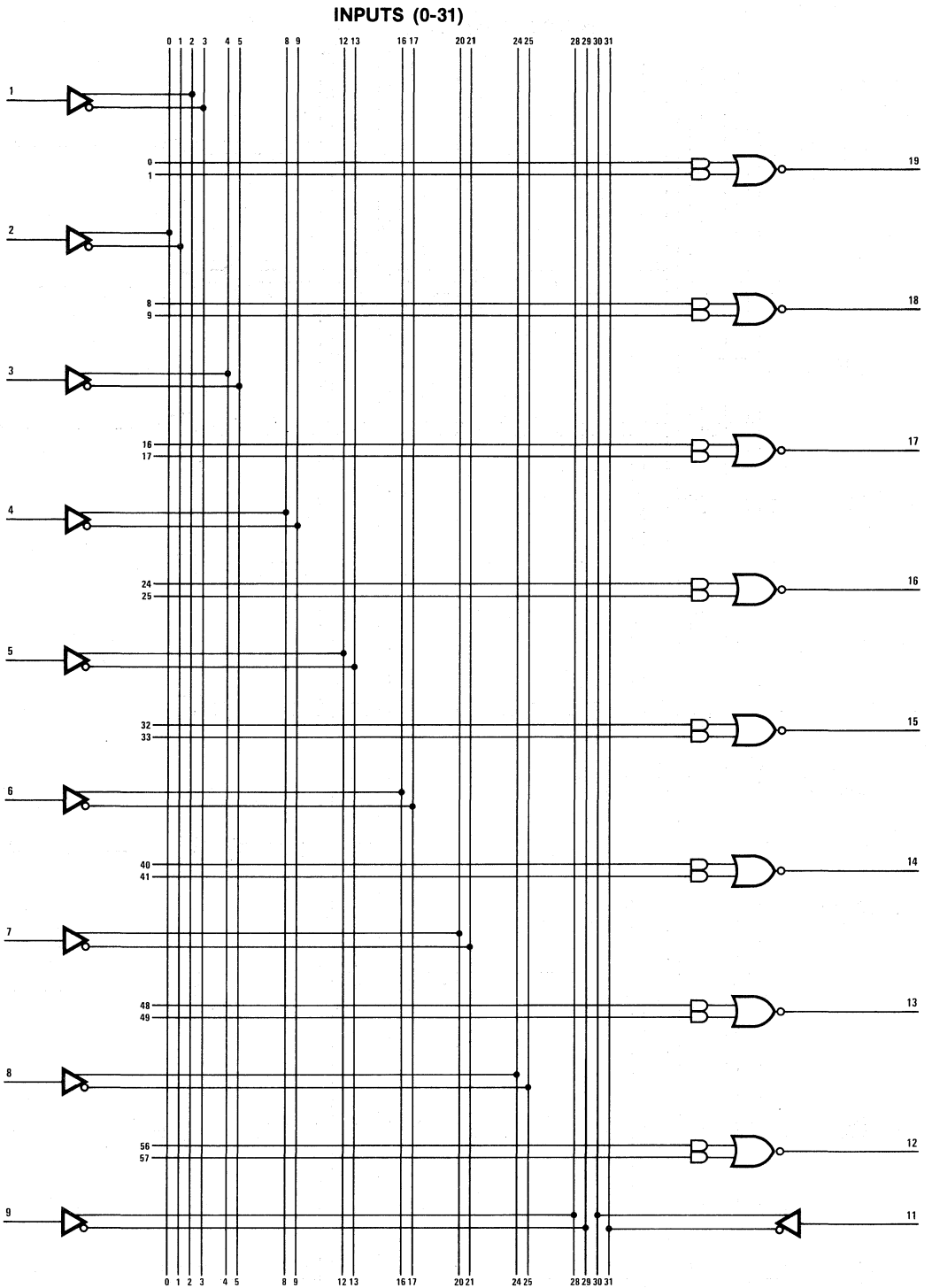
Logic Diagram PAL16H2



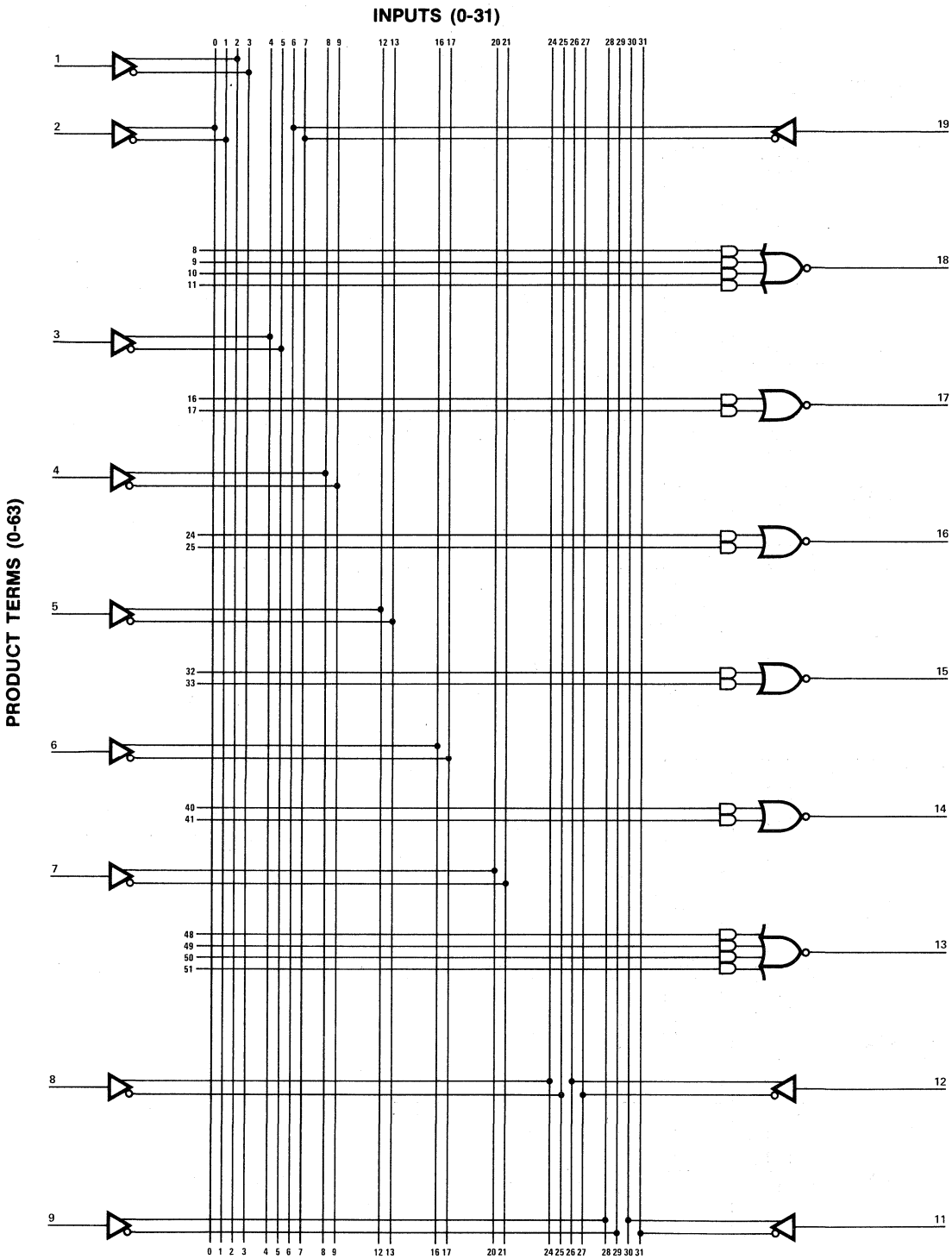
Logic Diagram PAL16C1



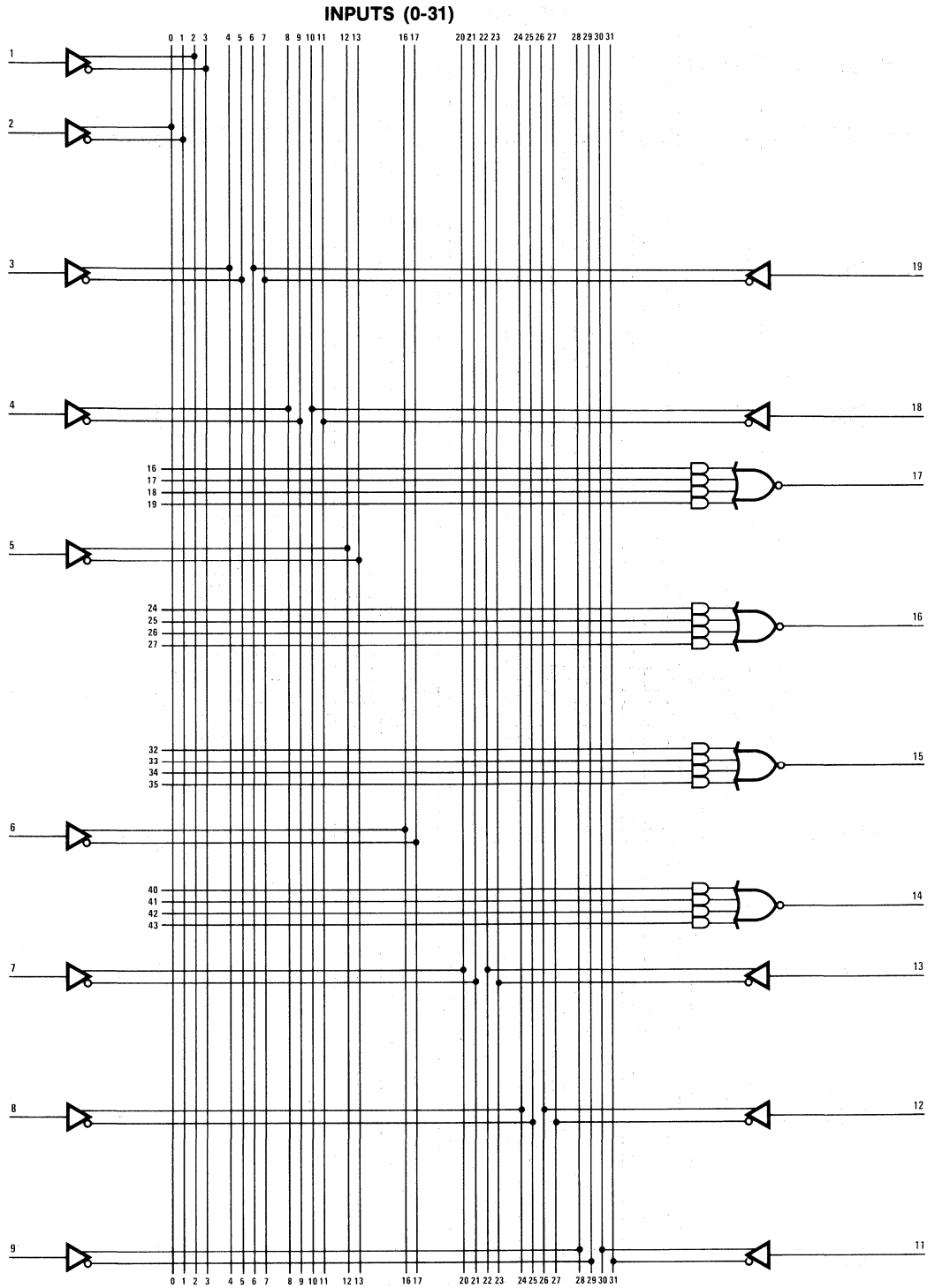
Logic Diagram PAL10L8



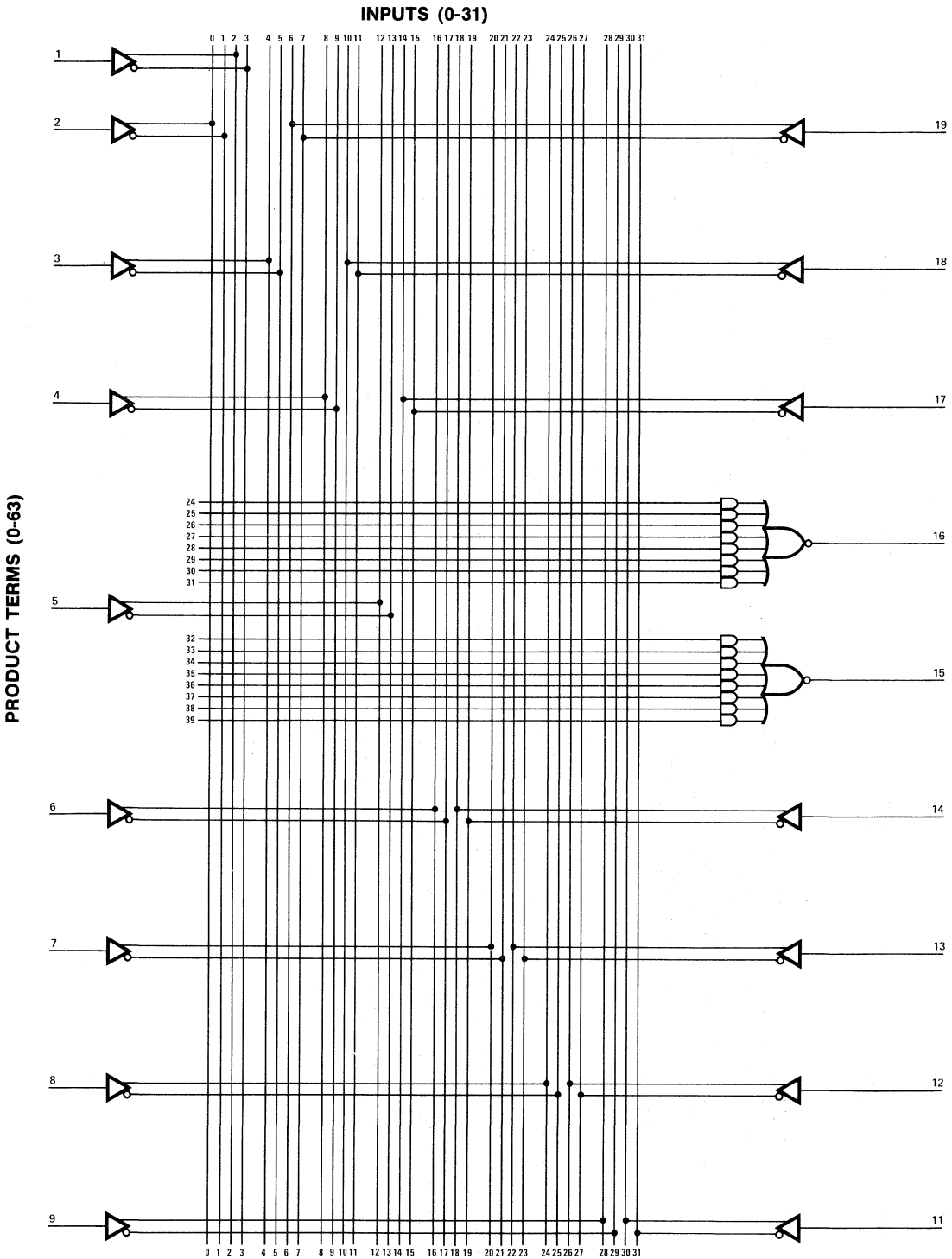
Logic Diagram PAL12L6



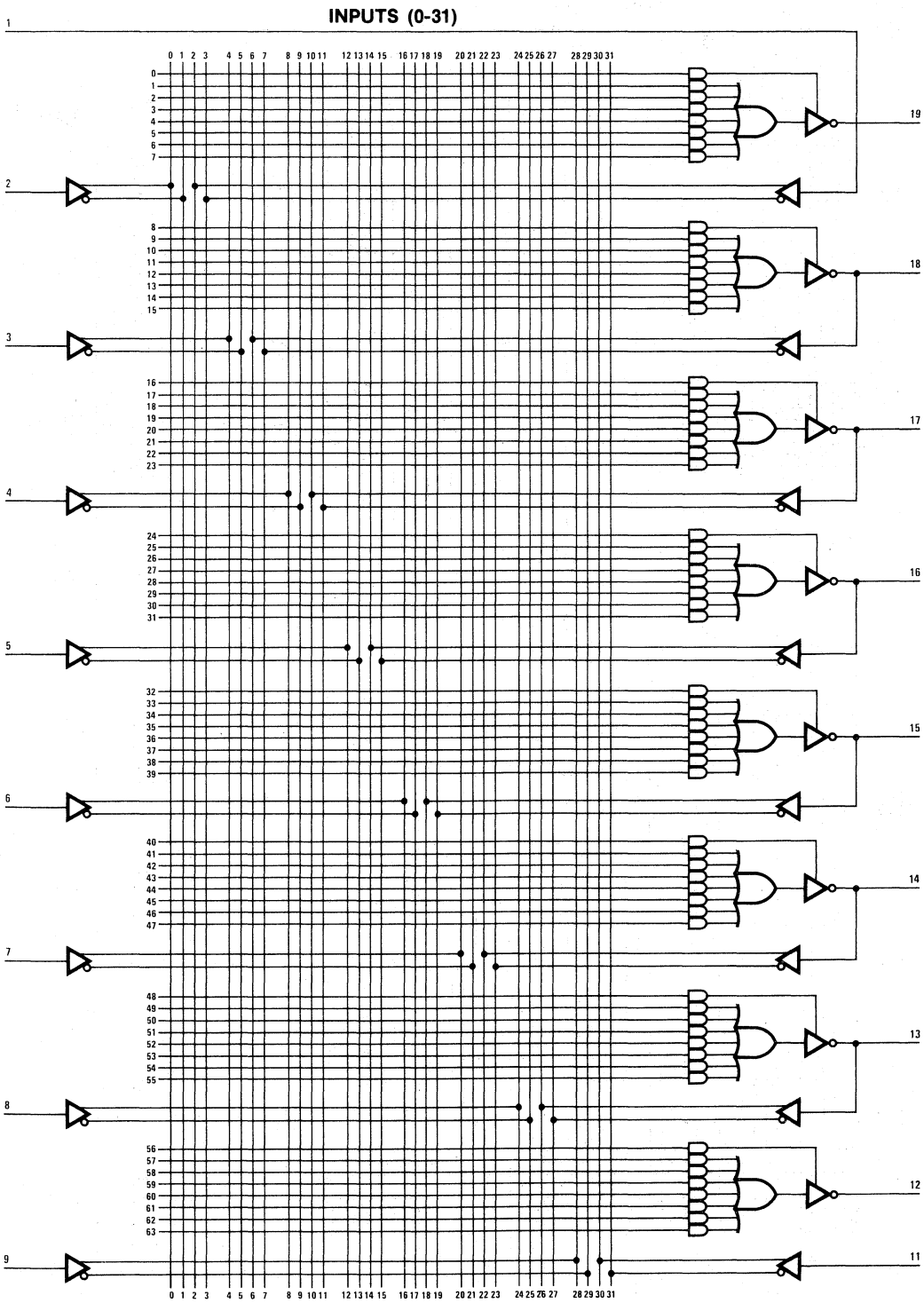
Logic Diagram PAL14L4



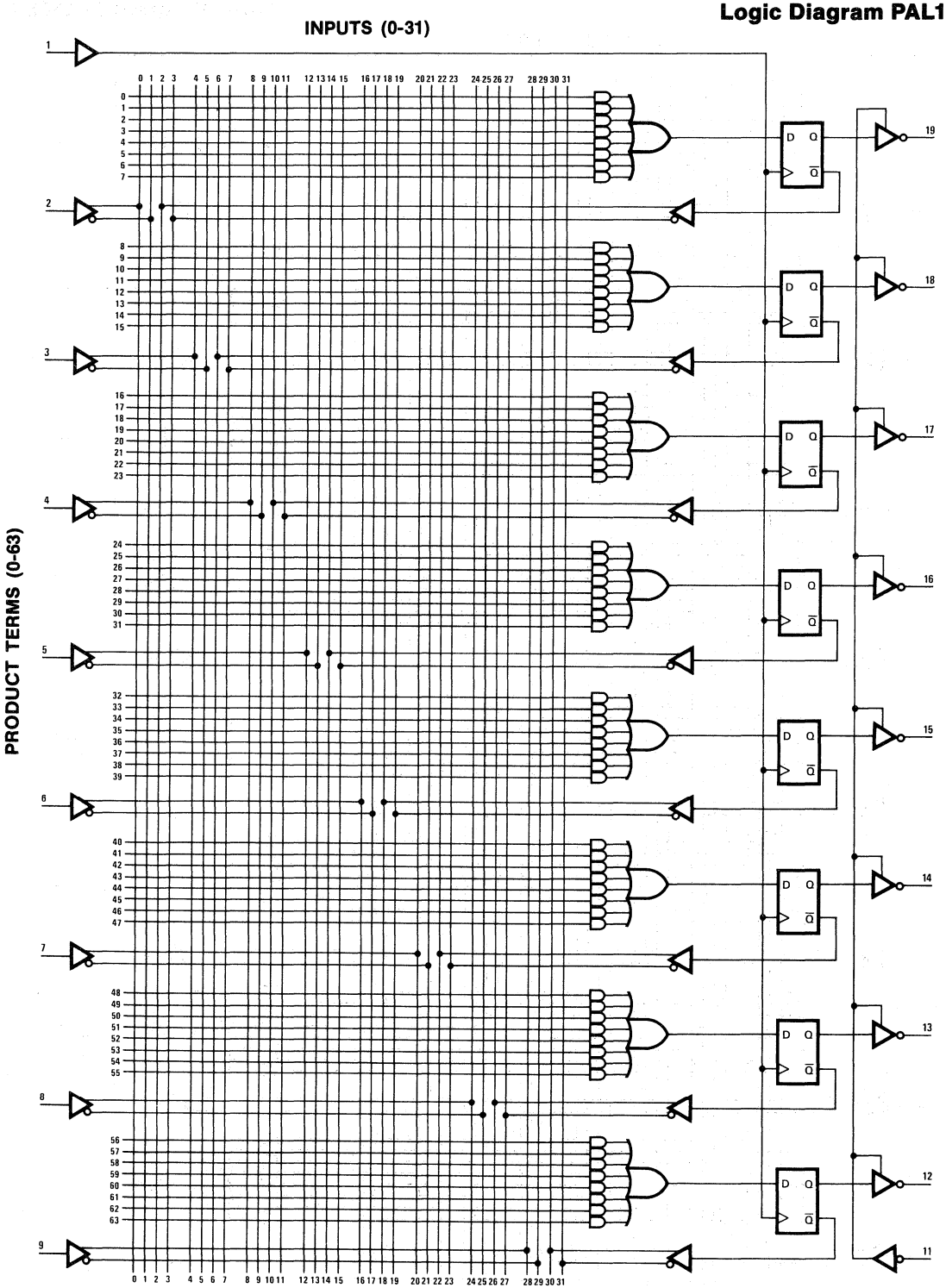
Logic Diagram PAL16L2



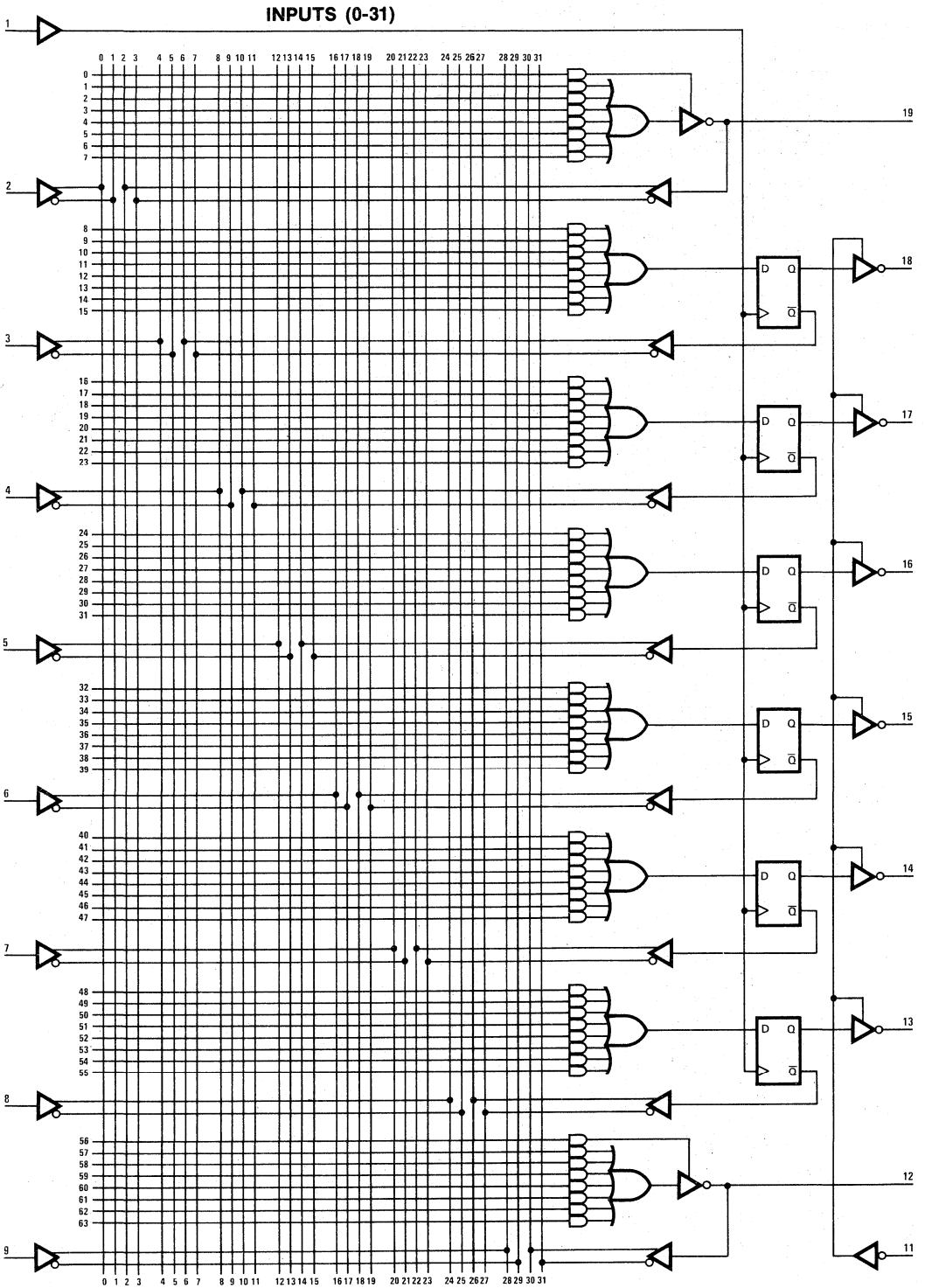
Logic Diagram PAL16L8



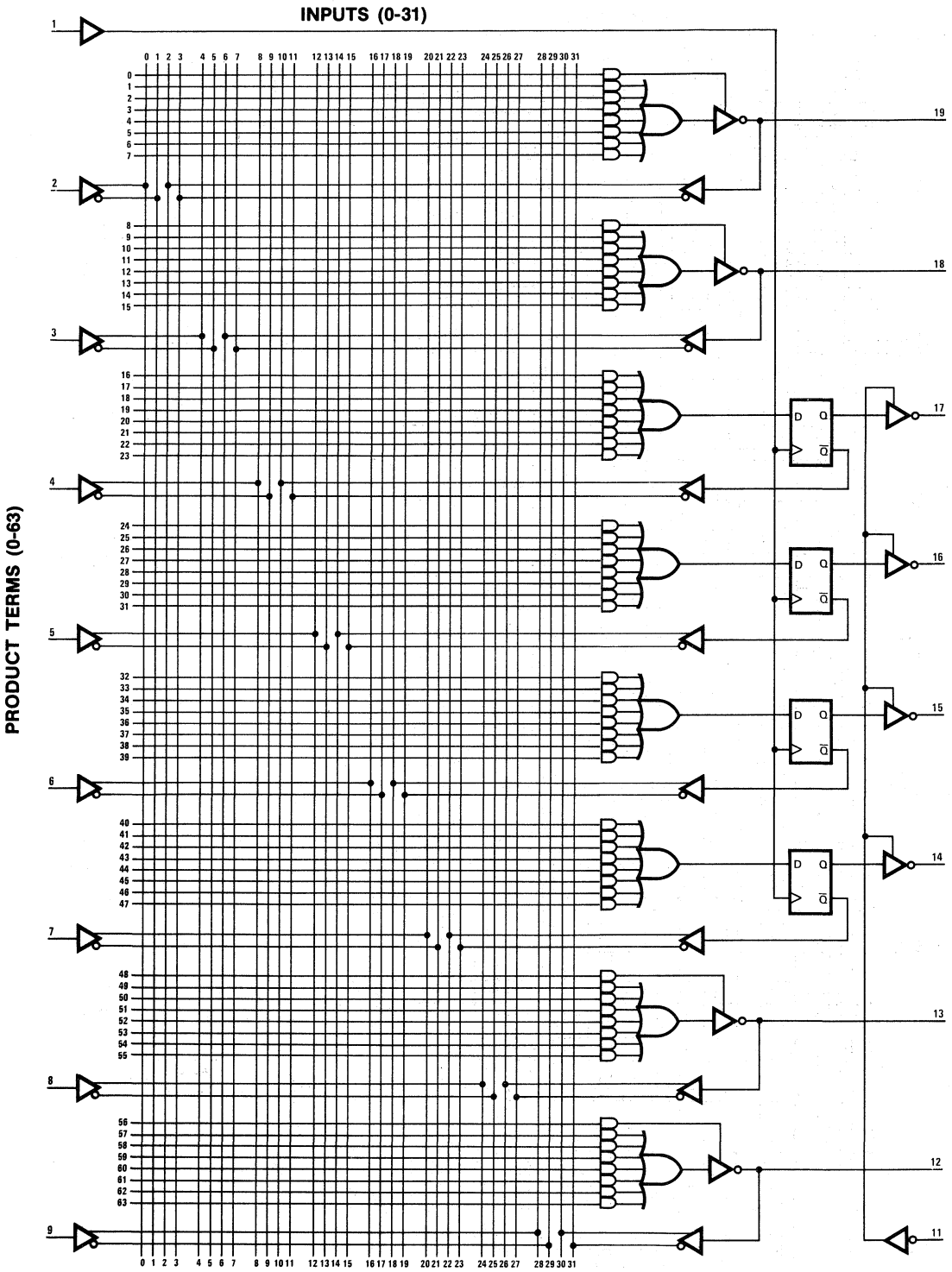
Logic Diagram PAL16R8



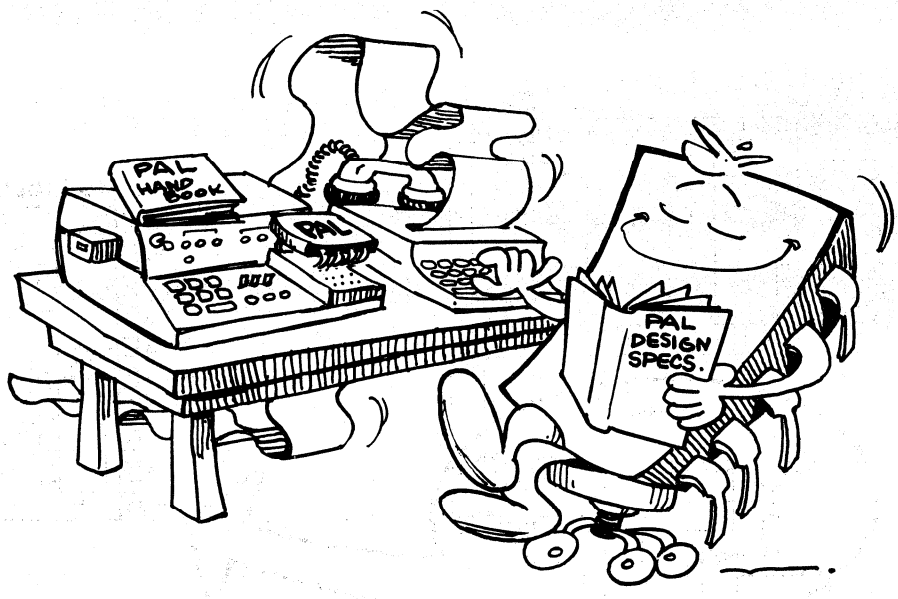
Logic Diagram PAL16R6



Logic Diagram PAL16R4



PAL Programming



Selecting the Right PAL

The 15 PAL part types offer a wide range of complexity to choose from. Starting with the PAL10H8 (10 inputs, 8 active high outputs), the first 9 PAL types can replace random SSI gate functions at about a 4 to 1 chip count reduction. With a variety of input/output pin ratios and Active High or Active Low outputs, this group, described as combinatorial, is designed to provide the Low Power Schottky (LS) fan-out and fan-in characteristics of 8 mA output sink (I_{OL}) for totem-pole outputs and 250 μA input loading (I_{IL}).

The next 6 PALS provide the additional features of three-state outputs, state sequencing, arithmetic, and programmable input/output pin ratios. The three-state outputs drive the standard LS output sink of 24 mA (I_{OL}), providing bus driving capability. These sequential PALs are ideal for replacing existing MSI and/or defining LSI functions not presently available.

Unused inputs should be tied to either V_{CC} or GND. The series resistor required for unused inputs on standard TTL is NOT required for PALs, thus using less parts.

Defining the Pinout

The first step in designing a PAL is selecting the Pinout. The example shown below shows a method for circling a section of conventionally drawn logic to define a boundary for a PAL function. This boundary will dictate a specific number of input pins and output pins. For the following example, 8 inputs and 6 outputs are required, well within the capability of the PAL10L8. Assignment of inputs and outputs to specific pins can be done using the PAL Logic Symbol as shown below.

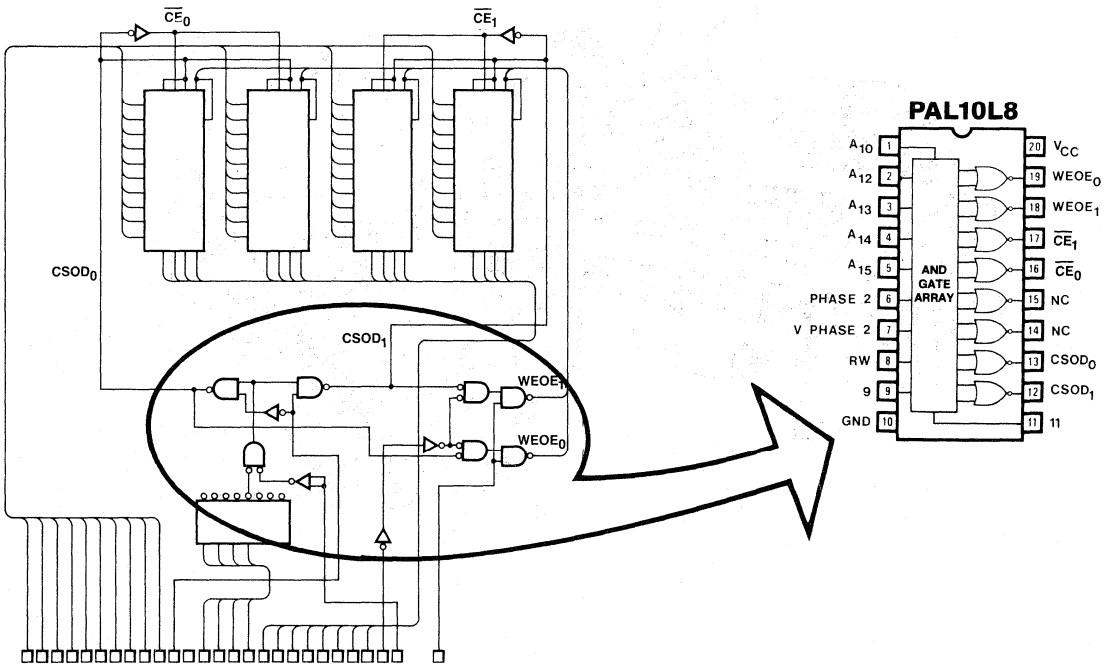
Specifying the Design

The next step is to generate a fuse pattern in order to program a PAL. The following two methods are commonly used for generating a fuse pattern.

PALASM:
Logic equations are entered as specified on page 6-31 and the fuse pattern is generated.

MANUAL CODING:
In this case logic equations or conventional logic diagram is translated into PAL logic diagram. This is accomplished by marking PAL logic diagrams with appropriate fuse interconnections for the desired logic transfer function. The PAL logic diagram is then transformed into PAL programming format. The programming format can be used to either enter data into the PAL Programmer manually, or to generate a tape using BHLF, BPNP or HEX format.

The two methods described above are explained in detail on the following pages. Page 6-29 gives the necessary information required to convert the conventional logic into PAL logic.



PAL Legend

Constants

LOW (L)	NEGATIVE (N)	ZERO (0)	GND	FALSE	×	FUSE NOT BLOWN
HIGH (H)	POSITIVE (P)	ONE (1)	V_{CC}	TRUE	–	FUSE BLOWN

Operators

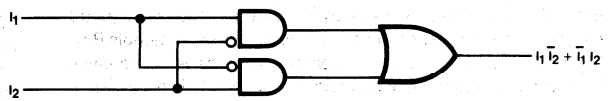
```
 =   EQUAL
:=   REPLACED BY FOLLOWING CLOCK
 /   COMPLEMENT
 *   AND, PRODUCT
 +   OR, SUM
:+:  XOR
:*:  XNOR
( )  CONDITIONAL THREE STATE, IF STATEMENT, ARITHMETIC
```

Equations

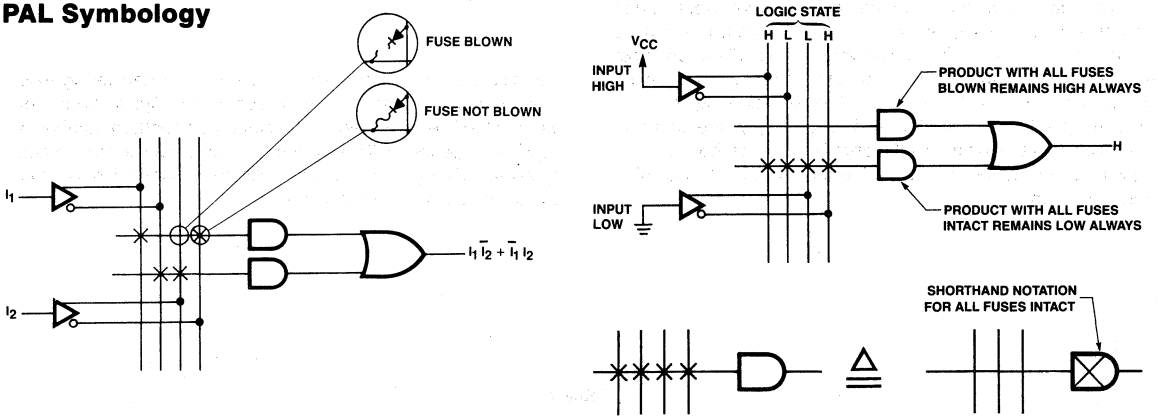
Standard $Q_1 = I_1 \overline{I_2} + \overline{I_1} I_2$

PALASM
```
O1 = I1*/I2 + /I1*I2
```

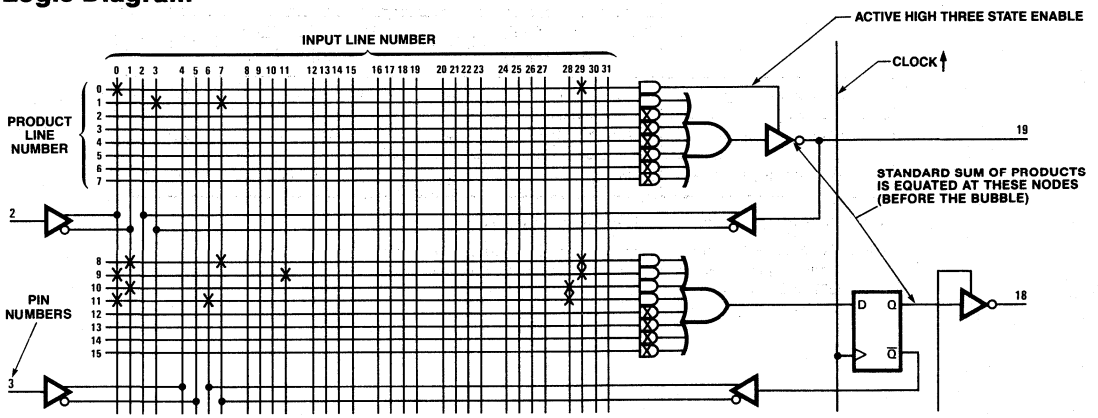
Conventional Symbology



PAL Symbology



PAL Logic Diagram



Phantom Fuse

Phantom fuse locations are those locations where a fuse does not exist. These are shown by the missing outputs, product terms or input lines in the Logic Diagrams on pages 6-14 thru 6-22. The PALs with phantom fuse locations appear to the PROM programmer as a partially programmed 512x4 PROM. As the programmer will expect to verify all 2048 locations, the PAL programming format must provide the expected pattern for verifying non-existent fuse nodes. When filling out the programming format, Table 1 should be used for phantom fuse locations. The following PALs have phantom fuses:

PAL10H8	PAL10L8
PAL12H6	PAL12L6
PAL14H4	PAL14L4
PAL16H2	PAL16L2
PAL16C1	

Documenting the PAL Design Specification

The PAL Design Specification is a recommended *data sheet* format for describing the function of a PAL once it has acquired the unique personality of a particular fuse pattern. A sample PAL Design Specification is shown on the next page. It contains the essential features of a data sheet including 1) Device Name, 2) Pin List, 3) Description, 4) Function Table and 5) Logic Diagram (on additional page). Two additional features not found in conventional data sheets are also included. First, is the author's name and the date. This information is standard on most engineering documents. Second, are the equations which define the PAL transfer function. The equations specify the precise operation of the PAL and, accordingly, are useful in understanding the function. Of higher importance, however, the equations are the key to automating the process of "designing your own chip."

PALASM

The equations in the PAL Design Specification, along with the PIN List and part number, contain the exact information necessary to generate PAL fuse patterns. Any computer can transform the spec into programming instructions in the form of paper tape or, preferably, RS232C voltage waveforms for direct input to PROM programmers. With a little help from your computer, your PALs can be designed, documented and programmed within minutes.

PALASM, for PAL Assembler, is a Fortran IV program which translates a PAL Design Specification into a PAL Fuse Pattern and PAL Programming Format (BHLF, BPNP or HEX). The flow chart on page 6-32 outlines the PALASM operation. PALASM source code is available to users on the following pages. Other source code media is available on request.

PROM programmer fuse patterns for VIRGIN PALs, using PALASM, are shown on pages 6-44 thru 6-46. Note that the unprogrammed locations are shown by an 'X' and phantom fuse locations are shown by '□' or '○', representing 'H' or 'L', respectively.

Monolithic Memories will assist customers in generating PAL programming formats. Equations sent to the Applications Department will be assembled and assigned a bit pattern number. A copy of the pattern will be returned for customer verification and approval. A programming order will be processed only after customer approval. (See page 6-80)

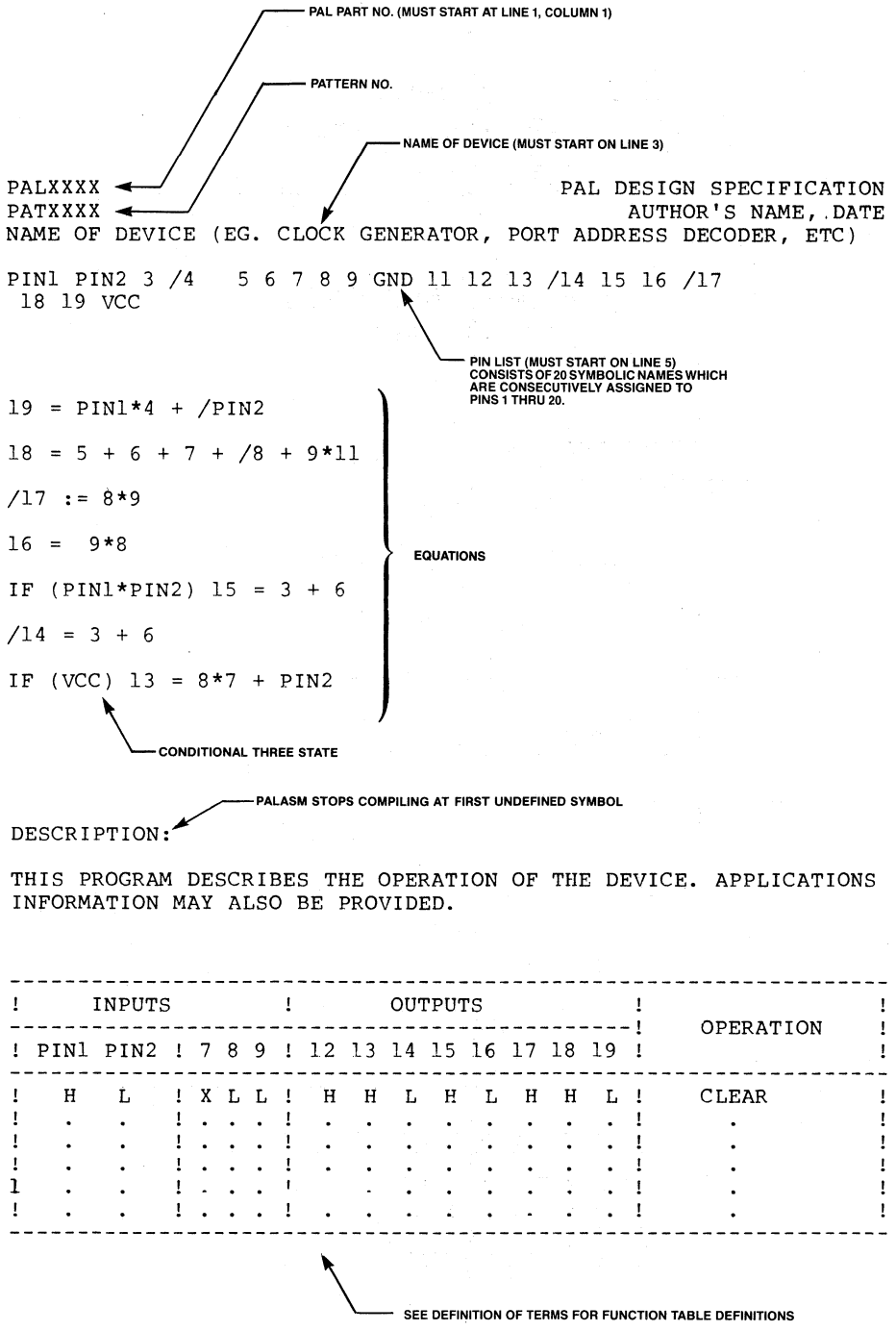
Table 1

	ACTIVE HIGH LOGIC		ACTIVE LOW LOGIC	
	(PAL 10H8, 12H6, 14H4, 16H2)	LEGEND	(PAL 10L8, 12L6, 14L4, 16L2)	LEGEND
1) Missing output	H (P,1)	⊕	L (N, O)	◆
2) Missing product	L (N, O)	◆	L (N, O)	◆
3) Missing input lines	H (P, 1)	⊕	H (P, 1)	⊕

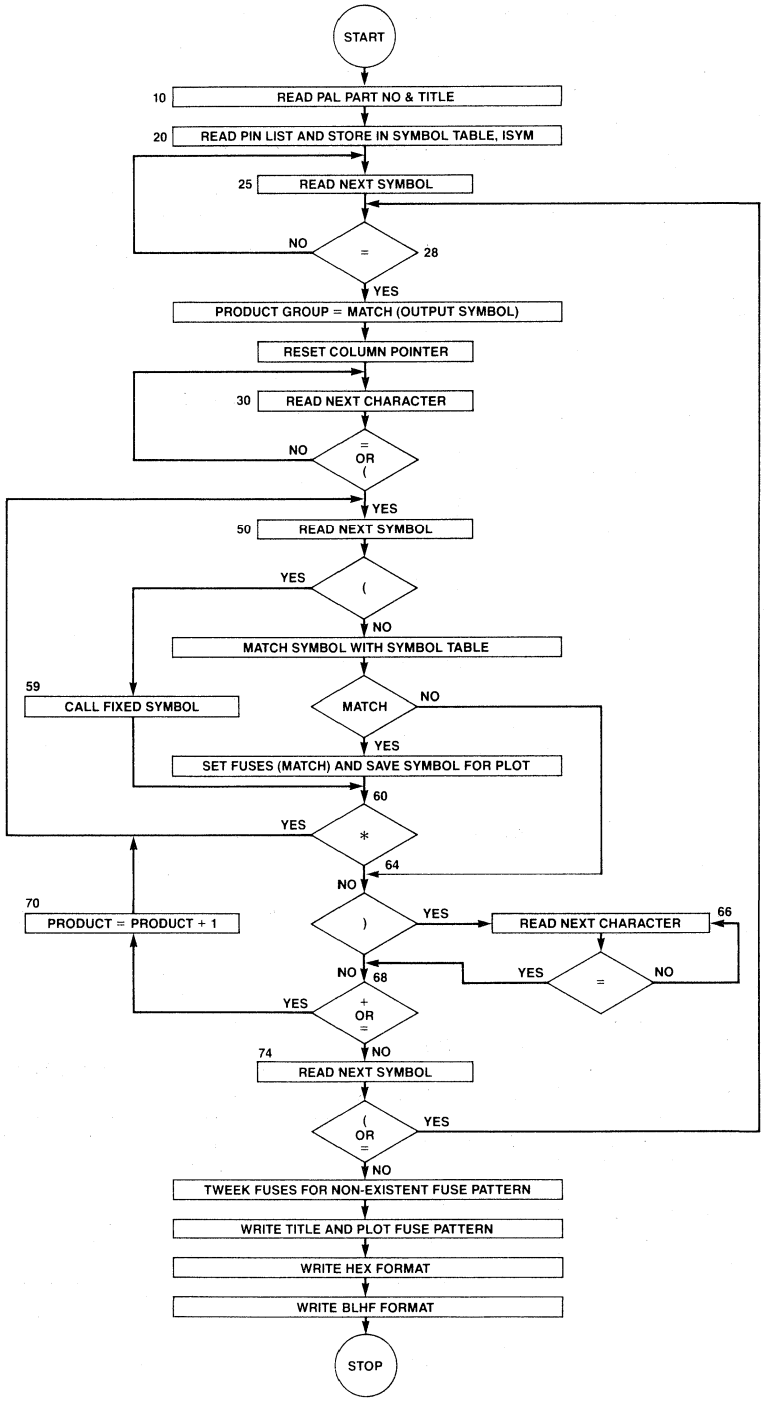
Note 1: Missing product term overrides missing input line.

Note 2: For PAL16C1, first half of the array (product terms 0-31) acts as active high logic and the second half of the array (product terms 32-63) acts as active low logic device.

Sample PAL Design Specification



PALASM Flow Chart



PALASM Source Code

```
C     P A L A S M   -   TRANSLATES SYMBOLIC EQUATIONS INTO PAL OBJECT
C                       CODE . FORMATTED FOR DIRECT INPUT TO STANDARD
C                       PROM PROGRAMMERS.
C
C                       INPUT:        PAL DESIGN SPECIFICATION ASSIGNED
C                                     TO DATA SET REFERENCE NUMBER 1
C
C                       OUTPUT:       FUSE PATTERN, HEX FORMAT, AND BHLF
C                                     FORMAT ON DATA SET REFERENCE
C                                     NUMBER 6.  COMMENTS ON DSRN 7 & 8
C
C                       PART NUMBER:  THE PAL PART NUMBER MUST
C                                     APPEAR IN COLUMN ONE OF LINE ONE
C
C                       PIN LIST:     20 SYMBOLIC PIN NAMES MUST APPEAR
C                                     STARTING ON LINE 5
C
C                       EQUATIONS:    STARTING FIRST LINE AFTER THE
C                                     PIN LIST IN THE FOLLOWING FORMS:
C
C                                        A = B*C + D
C
C                                        A := B*C + D
C
C                                        IF( A*B )  C = D + E
C
C                                        A2 := (A1:*:B1) + /C
C
C                                     BLANKS  ARE IGNORED
C
C                       OPERATORS:    =     EQUALITY
C                                     :=    REPLACED BY (AFTER CLOCK)
C                                     /     COMPLEMENT
C                                     *     AND, PRODUCT
C                                     +     OR,  SUM
C                                     :+:   EXCLUSIVE OR
C                                     :*:   EXCLUSIVE NOR
C                                     ()    CONDITIONAL THREE-STATE
C                                           OR FIXED SYMBOL
C
C                       FIXED SYMBOLS
C                       FOR PAL16X4
C                       AND PAL16A4
C                       ONLY:         (AN+/BN)          WHERE N = 0,1,2,3
C                                     (AN+BN)           FOR OUTPUT PINS
C                                     (AN)              17,16,15,14, RESP
C                                     (/AN+/BN)         A IS OUTPUT
C                                     (/BN)             B IS INPUT
C                                     (AN:+:BN)
C                                     (AN*/BN)
C                                     (/AN+BN)
C                                     (AN:*:BN)
C                                     (BN)
C                                     (AN*BN)
C                                     (/AN)
C                                     (/AN*/BN)
C                                     (/AN*BN)
C
C                       SUBROUTINES:  INITLZ,GETSYM,INCR,MATCH,FIXSYM,
C                                     TWEEK,PLOT,HEX,BHLF,MAP,SLIP
C
C                       FUNCTIONS:    IXLATE
C
C                       REV LEVEL:    J 1/16/80  JB,SK
C
C                       FINE PRINT:   MONOLITHIC MEMORIES TAKES NO
C                                     RESPONSIBILITY FOR THE OPERATION
C                                     OR MAINTENANCE OF THIS PROGRAM.
C                                     THE SOURCE CODE AS PRINTED HERE
C                                     PRODUCED THE OBJECT CODE OF THE
C                                     EXAMPLES IN THE APPLICATIONS
C                                     SECTION ON A NATIONAL CSS IBM
C                                     SYSTEM/370 FORTRAN IV(G).
C
C*************************************************************************
```

PALASM Source Code

```
C      MAIN PROGRAM
C
       COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT
       LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LFIRST,LFIX
       LOGICAL LFUSES(32,64),LPHASE(20),LBUF(20),LMATCH
       INTEGER TITLE(80),ILINE(80),ICOLUM,ISYM(8,20),IBUF(8,20),C,H,R,P,
     C         S,M,Q,IBLOW
       DATA LFUSES/2048*.FALSE./,ICOLUM/0/,L/'L'/,H/'H'/,N/'N'/,P/'P'/,
     C      C/'C'/,R/'R'/,M/'M'/,Q/'Q'/,IBLOW/0/,S/'S'/
C
       READ(1,10) INOAI,IOT,INOO,TITLE,ILINE
   10  FORMAT(3X,I2,A1,I1,//,80A1,//,80A1)
       CALL INITLZ(INOAI,IOT,INOO,ITYPE,LFUSES,ILINE,ICOLUM)
       DO 20 J=1,20
   20      CALL GETSYM(LPHASE,ISYM,J,ILINE,ICOLUM,LFIX)
           IF(.NOT.(LEQUAL.OR.LLEFT.OR.LAND.OR.LOR.OR.LRIGHT)) GO TO 25
               WRITE(7,23)
   23          FORMAT( ' PIN LIST ERROR, LESS THAN 20 SYMBOLS')
   25  CALL GETSYM(LBUF,IBUF,1,ILINE,ICOLUM,LFIX)
   28      IF(.NOT.LEQUAL) GO TO 25
           CALL MATCH(IMATCH,IBUF,ISYM)
           IF( (IMATCH.LT.12) .OR. (IMATCH.GT.19) ) GO TO 100
           I88PRO=(19-IMATCH)*8 + 1
           IF( IOT.EQ.C ) I88PRO=25
           ICOLUM=0
   30        CALL INCR(ILINE,ICOLUM,LFIX)
             IF( .NOT. (  LEQUAL.OR.LLEFT  ) ) GO TO 30
             IF(.NOT.LLEFT) CALL SLIP(LFUSES,I88PRO,INOAI,IOT,INOO,IBLOW)
           DO 70 I8PRO=1,16
               IPROD = I88PRO + I8PRO - 1
               LFIRST=.TRUE.
   50            CALL GETSYM(LBUF,IBUF,1,ILINE,ICOLUM,LFIX)
                 IF(LFIX) GO TO 59
                 CALL MATCH(IMATCH,IBUF,ISYM)
                 IF(IMATCH.EQ.0)  GO TO 100
                 IF(IMATCH.EQ.99) GO TO 64
                 IF(.NOT.LFIRST) GO TO 58
                     LFIRST=.FALSE.
                     DO 56 I=1,32
                         IBLOW = IBLOW + 1
   56                    LFUSES(I,IPROD)=.TRUE.
   58            IBUBL=0
                 IF(((     LPHASE(IMATCH)).AND.(.NOT.LBUF(1))).OR.
     C              ((.NOT.LPHASE(IMATCH)).AND.(     LBUF(1)))) IBUBL=1
                 IINPUT=IXLATE(IMATCH,ITYPE)+IBUBL
                 IF(IINPUT.LE.0) GO TO 60
                 IBLOW = IBLOW - 1
                 LFUSES(IINPUT,IPROD)=.FALSE.
                 CALL PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,.FALSE.,ITYPE)
                 GO TO 60
   59            CALL FIXSYM(LBUF,IBUF,ILINE,ICOLUM,LFIRST,LFUSES,IPROD,
     C           LFIX)
   60            IF(LAND) GO TO 50
   64          IF( .NOT.LRIGHT ) GO TO 68
   66            CALL INCR(ILINE,ICOLUM,LFIX)
                 IF( .NOT.LEQUAL )  GO TO 66
   68          IF(.NOT. (LOR.OR.LEQUAL) ) GO TO 74
   70          CONTINUE
   74      CALL GETSYM(LBUF,IBUF,1,ILINE,ICOLUM,LFIX)
           IF(LLEFT.OR.LEQUAL) GO TO 28
```

PALASM Source Code

```
  100 IF((IBUF(1,1).EQ.C).AND.(IBUF(2,1).EQ.R).AND.(IBUF(4,1).EQ.P)
     C  .AND.(IBUF(8,1).EQ.N))  GO TO 102
      WRITE(7,101) (IBUF(I,1),I=1,8),ILINE
  101 FORMAT(' ERROR SYMBOL = ',8A1,/,80A1,/)
  102 IF(ITYPE.LE.4) CALL TWEEK(ITYPE,IOT,LFUSES)
      WRITE(7,104) IBLOW
  104 FORMAT(' NUMBER OF FUSES BLOWN = ',I4)
      WRITE(8,106)
  106 FORMAT(' OPERATION CODES:  ',
     C 'P=PLOT H=HEX S=SHORT L=BHLF N=BPNF M=MAP Q=QUIT')
  108 WRITE(8,110)
  110 FORMAT(' ENTER OPERATION CODE')
      READ(5,120) IOP
  120 FORMAT(1A1)
      CALL IODC2
      IF(IOP.EQ.P) CALL PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,.TRUE.,ITYPE)
      IF(IOP.EQ.H) CALL HEX(LFUSES,H)
      IF(IOP.EQ.S) CALL HEX(LFUSES,S)
      IF(IOP.EQ.L) CALL BHLF(LFUSES,H,L)
      IF(IOP.EQ.N) CALL BHLF(LFUSES,P,N)
      IF(IOP.EQ.M) CALL MAP(LFUSES)
      CALL IODC4
      IF(IOP.NE.Q ) GO TO 108
      STOP
      END
C
C*************************************************************************
C
      SUBROUTINE INITLZ(INOAI,IOT,INOO,ITYPE,LFUSES,ILINE,ICOLUM,LFIX)
      INTEGER L,R,X,A
      LOGICAL LFIX
      DATA L/'L'/,R/'R'/,X/'X'/,A/'A'/
      IF( INOAI .LT. 16 )                          ITYPE = (INOAI/2) - 4
      IF( (INOAI .EQ. 16)                        ) ITYPE = 4
      IF( (INOAI .EQ. 16) .AND. (INOO .EQ. 8) )    ITYPE = 5
      IF( (IOT .EQ. R) .OR. (IOT .EQ. A) .OR. (IOT .EQ. X) ) ITYPE =6
      CALL INCR(ILINE,ICOLUM,LFIX)
      RETURN
      END
C
C*************************************************************************
C
      SUBROUTINE GETSYM(LPHASE,ISYM,J,ILINE,ICOLUM,LFIX)
      COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT
      LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LPHASE(20),LFIX
      INTEGER ILINE(80),ISYM(8,20),IBLANK
      DATA IBLANK/' '/
      LFIX=.FALSE.
      IF( .NOT.(LLEFT.OR.LAND.OR.LOR.OR.LEQUAL.OR.LRIGHT) )  GO TO 10
      CALL INCR(ILINE,ICOLUM,LFIX)
      IF(LLEFT) GO TO 60
   10 LPHASE(J)=( .NOT. LSLASH  )
      IF(LPHASE(J)) GO TO 15
      CALL INCR(ILINE,ICOLUM,LFIX)
   15 DO 20 I=1,8
   20     ISYM(I,J)=IBLANK
   25 DO 30 I=1,7
   30     ISYM(I,J)=ISYM(I+1,J)
      ISYM(8,J)=ILINE(ICOLUM)
      CALL INCR(ILINE,ICOLUM,LFIX)
      IF( LLEFT.OR.LBLANK.OR.LAND.OR.LOR.OR.LRIGHT.OR.LEQUAL ) GO TO 40
      GO TO 25
   40 CONTINUE
C     WRITE(7,50) (ISYM(I,J), I=1,8)
C  50 FORMAT(' ',8A1)
      RETURN
   60 LFIX=.TRUE.
      RETURN
      END
C
C*************************************************************************
C
```

PALASM Source Code

```
      SUBROUTINE INCR(ILINE,ICOLUM,LFIX)
      COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT
      LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LFIX
      INTEGER ILINE(80),IBLANK,ILEFT,IAND,IOR,ISLASH,IEQUAL,IRIGHT,
     C        ICOLON
      DATA IBLANK/' '/,ILEFT/'('/,IAND/'*'/,IOR/'+'/,
     C        ISLASH/'/'/,IEQUAL/'='/,IRIGHT/')'/,ICOLON/':'/
      LBLANK=.FALSE.
   10 ICOLUM=ICOLUM+1
      IF(ICOLUM.LE.79) GO TO 30
      READ(1,20,ERR=70,END=70) ILINE
      ICOLUM=1
   20 FORMAT(80A1)
   30 IF(  ILINE(ICOLUM) .EQ. IBLANK  )  LBLANK=.TRUE.
C     WRITE(7,50) ILINE(ICOLUM)
C  50 FORMAT(' .',1A1)
      IF( ( ILINE(ICOLUM).EQ.IBLANK ) .OR.
     C {(ILINE(ICOLUM).EQ.ICOLON).AND.(.NOT.LFIX))) GO TO 10
      LLEFT =(  ILINE(ICOLUM) .EQ.   ILEFT )
      LAND  =(  ILINE(ICOLUM) .EQ.   IAND  )
      LOR   =(  ILINE(ICOLUM) .EQ.    IOR  )
      LSLASH=(  ILINE(ICOLUM) .EQ.   ISLASH)
      LEQUAL=(  ILINE(ICOLUM) .EQ.   IEQUAL)
      LRIGHT=(  ILINE(ICOLUM) .EQ.   IRIGHT)
   60 RETURN
   70 LBLANK=.TRUE.
      RETURN
      END
C
C*************************************************************************
C
      SUBROUTINE MATCH(IMATCH,IBUF,ISYM)
      INTEGER IBUF(8,20),ISYM(8,20),C,A,R,Y
      LOGICAL LMATCH
      DATA C/'C'/,A/'A'/,R/'R'/,Y/'Y'/
      IMATCH=0
      DO 20 J=1,20
          LMATCH=.TRUE.
          DO 10 I=1,8
   10         LMATCH=LMATCH.AND.(IBUF(I,1).EQ.ISYM(I,J))
          IF(LMATCH) IMATCH=J
   20     CONTINUE
      IF((IBUF(3,1).EQ.C).AND.
     C   (IBUF(4,1).EQ.A).AND.
     C   (IBUF(5,1).EQ.R).AND.
     C   (IBUF(6,1).EQ.R).AND.
     C   (IBUF(7,1).EQ.Y))   IMATCH=99
      RETURN
      END
C
C*************************************************************************
C
      FUNCTION IXLATE(IMATCH,ITYPE)
      INTEGER ITABLE(20,6)
      DATA    ITABLE/
     C      3, 1, 5, 9,13,17,21,25,29,-1,31,-1,-1,-1,-1,-1,-1,-1,-1,-1,
     C      3, 1, 5, 9,13,17,21,25,29,-1,31,27,-1,-1,-1,-1,-1,-1, 7,-1,
     C      3, 1, 5, 9,13,17,21,25,29,-1,31,27,23,-1,-1,-1,-1,11, 7,-1,
     C      3, 1, 5, 9,13,17,21,25,29,-1,31,27,23,19,-1,-1,15,11, 7,-1,
     C      3, 1, 5, 9,13,17,21,25,29,-1,31,-1,27,23,19,15,11, 7,-1,-1,
     C     -1, 1, 5, 9,13,17,21,25,29,-1,-1,31,27,23,19,15,11, 7, 3,-1/
      IXLATE=ITABLE(IMATCH,ITYPE)
      RETURN
      END
C
C*************************************************************************
C
```

PALASM Source Code

```
      SUBROUTINE FIXSYM(LBUF,IBUF,ILINE,ICOLUM,LFIRST,LFUSES,IPROD,LFIX)
      LOGICAL LBUF(20),LFUSES(32,64),LFIRST,LMATCH,LFIX
      INTEGER IBUF(8,20),ILINE(80),FIXBUF(8),A,B,ISLASH,IOR,IAND,N,Q,
     C        N0,N1,N2,N3,IBLANK,IRIGHT,TABLE(5,14)
      DATA A/'A'/,B/'B'/,ISLASH/'/'/,IOR/'+'/,IBLANK/' '/,IRIGHT/')'/,
     C        IAND/'*'/,N/'N'/,Q/'Q'/,N0/'0'/,N1/'1'/,N2/'2'/,N3/'3'/,
     C       ICOLON/':'/,
     C        TABLE     /      ' ','A','+','/','B',' ',' ','A','+','B',
     C       ' ',' ',' ',' ','A','/','A','+','/','B',' ',' ',' ','/','B',
     C       'A',':','+',':','B',' ','A','*','/','B',' ','/','A','+','B',
     C       'A',':','*',':','B',' ',' ',' ',' ','B',' ',' ','A','*','B',
     C       ' ',' ',' ','/','A','/','A','*','/','B',' ','/','A','*','B'/
      IINPUT=0
      DO 20 I=1,8
          IBUF(I,1)=IBLANK
   20     FIXBUF(I)=IBLANK
   21 CALL INCR(ILINE,ICOLUM,LFIX)
      I=ILINE(ICOLUM)
      IF(I.EQ.IRIGHT) GO TO 40
      IF(I.EQ.N0) IINPUT=8
      IF(I.EQ.N1) IINPUT=12
      IF(I.EQ.N2) IINPUT=16
      IF(I.EQ.N3) IINPUT=20
      DO 24 J=1,7
   24     IBUF(J,1)=IBUF(J+1,1)
      IBUF(8,1)=I
      IF(.NOT. ( (I.EQ.A).OR.(I.EQ.B).OR.(I.EQ.ISLASH).OR.(I.EQ.IOR)
     C        .OR.(I.EQ.IAND).OR.(I.EQ.ICOLON) ) )  GO TO 21
      DO 30 I=1,4
   30     FIXBUF(I)=FIXBUF(I+1)
      FIXBUF(5)=ILINE(ICOLUM)
      GO TO 21
   40 IMATCH=0
      DO 60 J=1,14
          LMATCH=.TRUE.
          DO 50 I=1,5
   50         LMATCH=LMATCH .AND. ( FIXBUF(I).EQ.TABLE(I,J) )
   60     IF(LMATCH) IMATCH=J
      IF(IMATCH.EQ.0) GO TO 100
      IF(.NOT.LFIRST) GO TO 85
          LFIRST=.FALSE.
          DO 80 I=1,32
   80         LFUSES(I,IPROD)=.TRUE.
   85 DO 90 I=1,4
      IF( (IMATCH-7).GT.0 ) LFUSES(IINPUT+I,IPROD)=.FALSE.
      IF( (IMATCH-7).GT.0 ) IMATCH=IMATCH-8
   90 IMATCH=IMATCH+IMATCH
      LBUF(1)=.TRUE.
      CALL PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,.FALSE.,ITYPE)
  100 LFIX=.FALSE.
      CALL INCR(ILINE,ICOLUM,LFIX)
      RETURN
      END
C
C*******************************************************************************
C
      SUBROUTINE IODC2
C*** THIS ROUTINE IS OPTIONAL.  IT MAY BE USED TO TURN PERIPHERALS ON.
      INTEGER DC2,BEL
      DATA DC2/Z12000000/,BEL/Z2F000000/
      WRITE(6,10) DC2,BEL
   10 FORMAT(' ',2A1)
      RETURN
      END
C
C*******************************************************************************
C
```

PALASM Source Code

```
      SUBROUTINE PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,LDUMP,ITYPE)
      INTEGER IBUF(8,20),IOUT(64),IBLANK,IAND,IOR,ISLASH,IDASH,X,
     C        ISAVE(64,32),TITLE(80)
      DATA IBLANK/' '/,IAND/'*'/,ISAVE/2048*' '/,
     C        IOR/'+'/,ISLASH/'/'/,X/'X'/,IDASH/'-'/
      LOGICAL LBUF(20),LFUSES(32,64),LDUMP
      IF(LDUMP) GO TO 60
      IF(ISAVE(IPROD,1).NE.IBLANK) RETURN
      IF(  LBUF(1)  )  GO TO 5
      DO 30 J=1,31
   30     ISAVE(IPROD,J)=ISAVE(IPROD,J+1)
      ISAVE(IPROD,32)=ISLASH
    5 DO 20 I=1,8
        IF(  ISAVE(IPROD,1).NE.IBLANK  )  RETURN
         IF(  IBUF(I,1) .EQ. IBLANK  )  GO TO 20
         DO 10 J=1,31
   10         ISAVE(IPROD,J)=ISAVE(IPROD,J+1)
        ISAVE(IPROD,32)=IBUF(I,1)
   20   CONTINUE
      IF(ISAVE(IPROD,1).NE.IBLANK) RETURN
   40 DO 50 J=1,31
   50     ISAVE(IPROD,J)=ISAVE(IPROD,J+1)
      ISAVE(IPROD,32)=IAND
      RETURN
   60 WRITE(6,62) TITLE
   62 FORMAT(////,' ',80A1,//,
     C '                    11 1111 1111 2222 2222 2233',/,
     C '    0123 4567 8901 2345 6789 0123 4567 8901',/)
      DO 100 I88PRO=1,57,8
          DO 94 I8PRO=1,8
              IPROD=I88PRO+I8PRO-1
              ISAVE(IPROD,32)=IBLANK
              DO 70 I=1,32
                  IF(  ISAVE(IPROD,1) .NE. IBLANK  )  GO TO 70
                  DO 65 J=1,31
   65                 ISAVE(IPROD,J)=ISAVE(IPROD,J+1)
                  ISAVE(IPROD,32)=IBLANK
   70             CONTINUE
              DO 80 I=1,32
                  IOUT(I)=X
                  IF(  LFUSES(I,IPROD) )  IOUT(I)=IDASH
                  IOUT(I+32)=ISAVE(IPROD,I)
   80         CONTINUE
              IF( ITYPE .LE. 4 )  CALL FANTOM(ITYPE,IOUT,IPROD,I8PRO)
              IPROD=IPROD-1
              WRITE(6,90) IPROD,IOUT
   90         FORMAT(' ',I2,8(' ',4A1),' ',32A1)
   94         CONTINUE
          WRITE(6,96)
   96     FORMAT(1X)
  100     CONTINUE
      WRITE(6,110)
  110 FORMAT(/,
     C' LEGEND:  X : FUSE NOT BLOWN (L,N,0)   - : FUSE BLOWN   (H,P,1)')
      IF (ITYPE.LE.4) WRITE(6,111)
  111 FORMAT(
     C'           0 : PHANTOM FUSE   (L,N,0)   O : PHANTOM FUSE (H,P,1)')
      WRITE(6,112)
  112 FORMAT(////)
      RETURN
      END
C
C*******************************************************************************
C
```

PALASM Source Code

```
      SUBROUTINE HEX(LFUSES,IOP)
      LOGICAL LFUSES(32,64)
      INTEGER ITEMP(64),S,H,IOP
      DATA STX/Z02000000/,BEL/Z2F000000/,SOH/Z01000000/,
     C     H/'H'/,S/'S'/
      IF(IOP.EQ.H) WRITE(6,10)
   10 FORMAT(//,'                                                .',//)
C***** NOTE: SOME PROM PROGRAMMERS NEED A START CHARACTER.
C*****       THIS PROGRAM OUTPUTS AN STX FOR THE DATA I/O MODEL 9
C*****         (USE SOH FOR MODEL 5)
      WRITE(6,5) BEL,BEL,BEL,BEL,BEL,BEL,BEL,STX,SOH
    5 FORMAT(9A1)
      DO 40 I=1,33,32
      INC=I-1
        DO 40 IPROD=1,7,2
          DO 20 J=1,2
              DO 20 IINPUT=1,32
              IHEX=0
              IF(LFUSES(IINPUT,IPROD + J-1 + 0+INC)) IHEX=IHEX+1
              IF(LFUSES(IINPUT,IPROD + J-1 + 8+INC)) IHEX=IHEX+2
              IF(LFUSES(IINPUT,IPROD + J-1 +16+INC)) IHEX=IHEX+4
              IF(LFUSES(IINPUT,IPROD + J-1 +24+INC)) IHEX=IHEX+8
   20         ITEMP(IINPUT + 32*(J-1) )=IHEX
        IF(IOP.EQ.H) WRITE(6,60) ITEMP
   40   IF(IOP.EQ.S) WRITE(6,61) ITEMP
   60   FORMAT(' ',32(Z1,' '),'.',/,' ',32(Z1,' '),'.')
   61   FORMAT(' ',64Z1)
      IF(IOP.EQ.H) WRITE(6,70)
   70 FORMAT(' ',//,'                                                .',//)
      RETURN
      END
C
C*************************************************************************
C
      SUBROUTINE BHLF(LFUSES,H,L)
      LOGICAL LFUSES(32,64)
      INTEGER ITEMP(4,8),L,H
      WRITE(6,10)
   10 FORMAT(//,'                                                .',//)
      DO 20 I=1,33,32
      INC=I-1
        DO 20 IPROD=1,8
            DO 20 J=1,25,8
              DO 15 K=1,8
                IINPUT=J+K-1
                ITEMP(1,K)=L
                ITEMP(2,K)=L
                ITEMP(3,K)=L
                ITEMP(4,K)=L
                IF(LFUSES(IINPUT,IPROD+ 0+INC)) ITEMP(4,K)=H
                IF(LFUSES(IINPUT,IPROD+ 8+INC)) ITEMP(3,K)=H
                IF(LFUSES(IINPUT,IPROD+16+INC)) ITEMP(2,K)=H
                IF(LFUSES(IINPUT,IPROD+24+INC)) ITEMP(1,K)=H
   15           CONTINUE
   20         WRITE(6,30) ITEMP
   30         FORMAT(' ',8('B',4A1,'F '))
      WRITE(6,10)
      RETURN
      END
C
C*************************************************************************
C
      SUBROUTINE IODC4
C*** THIS ROUTINE IS OPTIONAL.  IT MAY BE USED TO TURN PERIPHERALS OFF.
      INTEGER DC3,DC4,BEL
      DATA DC3/Z37000000/,DC4/Z3C000000/,BEL/Z2F000000/
      WRITE(6,10) BEL,DC3,DC4
   10 FORMAT(' ',3A1)
      RETURN
      END
C
C*************************************************************************
C
```

PALASM Source Code

```
      SUBROUTINE TWEEK(ITYPE,IOT,LFUSES)
      INTEGER L,C
      LOGICAL LFUSES(32,64)
      DATA L/'L'/,C/'C'/
      IF(ITYPE.GE.4) GO TO 20
      DO 10 IPROD=1,64
          LFUSES(15,IPROD)=.TRUE.
          LFUSES(16,IPROD)=.TRUE.
          LFUSES(19,IPROD)=.TRUE.
          LFUSES(20,IPROD)=.TRUE.
          IF(ITYPE.GE.3) GO TO 10
          LFUSES(11,IPROD)=.TRUE.
          LFUSES(12,IPROD)=.TRUE.
          LFUSES(23,IPROD)=.TRUE.
          LFUSES(24,IPROD)=.TRUE.
          IF(ITYPE.GE.2) GO TO 10
          LFUSES( 7,IPROD)=.TRUE.
          LFUSES( 8,IPROD)=.TRUE.
          LFUSES(27,IPROD)=.TRUE.
          LFUSES(28,IPROD)=.TRUE.
   10     CONTINUE
      DO 18 IINPUT=7,28
          DO 12 IPROD=1,57,8
              LFUSES(IINPUT,IPROD+4)=.FALSE.
              LFUSES(IINPUT,IPROD+5)=.FALSE.
              LFUSES(IINPUT,IPROD+6)=.FALSE.
   12         LFUSES(IINPUT,IPROD+7)=.FALSE.
          IF(ITYPE.GE.3) GO TO 18
          DO 14 IPROD=17,41,8
              LFUSES(IINPUT,IPROD+2)=.FALSE.
   14         LFUSES(IINPUT,IPROD+3)=.FALSE.
          IF(ITYPE.GE.2) GO TO 18
          DO 16 IPROD=1,57,8
              LFUSES(IINPUT,IPROD+2)=.FALSE.
   16         LFUSES(IINPUT,IPROD+3)=.FALSE.
   18 CONTINUE
   20 IF( (ITYPE.EQ.1) .OR. ((ITYPE.EQ.4).AND.(IOT.EQ.L)) ) GO TO 100
      DO 99 IINPUT=1,32
          DO 30 IPROD=1,8
              LFUSES(IINPUT,IPROD+ 0)= (IOT.NE.L)
   30         IF(IOT.NE.C) LFUSES(IINPUT,IPROD+56)= (IOT.NE.L)
          IF(ITYPE.LE.2) GO TO 99
          DO 40 IPROD=1,8
              LFUSES(IINPUT,IPROD+ 8)= (IOT.NE.L)
   40         IF(IOT.NE.C) LFUSES(IINPUT,IPROD+48)= (IOT.NE.L)
          IF(ITYPE.LE.3) GO TO 99
          DO 50 IPROD=1,8
              LFUSES(IINPUT,IPROD+16)= (IOT.NE.L)
   50         IF(IOT.NE.C) LFUSES(IINPUT,IPROD+40)= (IOT.NE.L)
   99     CONTINUE
  100 RETURN
      END
C
C*******************************************************************************
C
      SUBROUTINE SLIP(LFUSES,I88PRO,INOAI,IOT,INOO,IBLOW)
      LOGICAL LFUSES(32,64)
      INTEGER R
      DATA R/'R'/
      IF( (INOAI.LT.16) .OR. (INOO.LT.4) .OR.
     C    ( (IOT.EQ.R).AND.(INOO.EQ.8) ) .OR.
     C    ( (I88PRO.GE. 9).AND.(I88PRO.LE.49).AND.(INOO.EQ.6) ) .OR.
     C    ( (I88PRO.GE.17).AND.(I88PRO.LE.41).AND.(INOO.EQ.4) ) ) RETURN
      DO 10 I=1,32
      IBLOW = IBLOW + 1
   10 LFUSES(I,I88PRO) = .TRUE.
      I88PRO = I88PRO + 1
      RETURN
      END
C
C*******************************************************************************
C
```

PALASM Source Code

```
      SUBROUTINE MAP(LFUSES)
      LOGICAL LFUSES(32,64)
      INTEGER X,D,ILINE(16),ITABLE(32)
      DATA X/'X'/,D/'-'/,
     C ITABLE/17,16,19,18,21,20,23,22,25,24,27,26,29,28,31,30,
     C        13,12,15,14, 9, 8,11,10, 5, 4, 7, 6, 1, 0, 3, 2/
      WRITE(6,10)
   10 FORMAT(     '                    INPUT',//,
     C            '          11 11 22 22 22 22 22 33',/,
     C            '          76 98 10 32 54 76 98 10',//,
     C            '          11 11    11             ',/,
     C            ' PRODUCT 32 54 98 10 54 76 10 32',/ )
      IPROD=7
      IDELTA = -1
      DO 50  I=1,2
          DO 40 J=1,4
              DO 30 K=1,4
                  DO 20 L=1,16
                      ILINE(L)=X
   20                 IF( LFUSES(ITABLE(L)+1 ,IPROD+1 ) ) ILINE(L)=D
                  WRITE(6,21) IPROD,ILINE
   21             FORMAT('    ',I2,'     ',8(2A1,' ') )
                  DO 22 L=1,16
                      ILINE(L)=X
   22                 IF( LFUSES(ITABLE(L+16)+1 ,IPROD+1 ) ) ILINE(L)=D
                  WRITE(6,21) IPROD,ILINE
                  IPROD = IPROD + IDELTA
                  DO 23 L=1,16
                      ILINE(L)=X
   23                 IF( LFUSES(ITABLE(L+16)+1 ,IPROD+1 ) ) ILINE(L)=D
                  WRITE(6,21) IPROD,ILINE
                  DO 24 L=1,16
                      ILINE(L)=X
   24                 IF( LFUSES(ITABLE(L)+1 ,IPROD+1 ) ) ILINE(L)=D
                  WRITE(6,21) IPROD,ILINE
   30             IPROD = IPROD + IDELTA
              WRITE(6,29)
   29         FORMAT(' ')
   40         IPROD  = IPROD + 8*(1-IDELTA)
          IPROD  = 32
   50     IDELTA = +1
      WRITE(6,29)
      WRITE(6,29)
      RETURN
      END
C
C*************************************************************************
C
      SUBROUTINE FANTOM(ITYPE,IOUT,IPROD,I8PRO)
      INTEGER ITYPE,IOUT(64),IPROD,I8PRO,X,IDASH,FX,FIDASH
      DATA X/'X'/,IDASH/'-'/,FX/'0'/,FIDASH/'O'/
      DO 10 I=1,32
          IF( IOUT(I).EQ.X     ) IOUT(I)=FX
   10     IF( IOUT(I).EQ.IDASH ) IOUT(I)=FIDASH
      IF((ITYPE.EQ.4).AND.((IPROD.LE.24).OR.(IPROD.GE.41))) GO TO 100
      IF((ITYPE.EQ.3).AND.((IPROD.LE.16).OR.(IPROD.GE.45))) GO TO 100
      IF((ITYPE.EQ.2).AND.((IPROD.LE. 8).OR.(IPROD.GE.53))) GO TO 100
      IF((ITYPE.LE.3).AND.(I8PRO.GE.5)) GO TO 100
      IF((ITYPE.LE.2).AND.(IPROD.GE.19).AND.(IPROD.LE.48).AND.
     C   (I8PRO.GE.3)) GO TO 100
      IF((ITYPE.EQ.1).AND.(I8PRO.GE.3)) GO TO 100
      DO 50 I=1,32
        IF(((I.EQ.15).OR.(I.EQ.16).OR.(I.EQ.19).OR.(I.EQ.20)).AND.
     C    (ITYPE.LE.3)) GO TO 50
        IF(((I.EQ.11).OR.(I.EQ.12).OR.(I.EQ.23).OR.(I.EQ.24)).AND.
     C    (ITYPE.LE.2)) GO TO 50
        IF(((I.EQ. 7).OR.(I.EQ. 8).OR.(I.EQ.27).OR.(I.EQ.28)).AND.
     C    (ITYPE.LE.1)) GO TO 50
        IF(IOUT(I).EQ.FX    ) IOUT(I)=X
        IF(IOUT(I).EQ.FIDASH) IOUT(I)=IDASH
   50 CONTINUE
  100 RETURN
      END
C
C*************************************************************************
C
```

PROM Programmer Virgin Fuse Patterns

PAL10H8

```
                    11 1111 1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
 1 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
 2 0000 0000 0000 0000 0000 0000 0000 0000
 3 0000 0000 0000 0000 0000 0000 0000 0000
 4 0000 0000 0000 0000 0000 0000 0000 0000
 5 0000 0000 0000 0000 0000 0000 0000 0000
 6 0000 0000 0000 0000 0000 0000 0000 0000
 7 0000 0000 0000 0000 0000 0000 0000 0000

 8 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
 9 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
10 0000 0000 0000 0000 0000 0000 0000 0000
11 0000 0000 0000 0000 0000 0000 0000 0000
12 0000 0000 0000 0000 0000 0000 0000 0000
13 0000 0000 0000 0000 0000 0000 0000 0000
14 0000 0000 0000 0000 0000 0000 0000 0000
15 0000 0000 0000 0000 0000 0000 0000 0000

16 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
17 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
18 0000 0000 0000 0000 0000 0000 0000 0000
19 0000 0000 0000 0000 0000 0000 0000 0000
20 0000 0000 0000 0000 0000 0000 0000 0000
21 0000 0000 0000 0000 0000 0000 0000 0000
22 0000 0000 0000 0000 0000 0000 0000 0000
23 0000 0000 0000 0000 0000 0000 0000 0000

24 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
25 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
26 0000 0000 0000 0000 0000 0000 0000 0000
27 0000 0000 0000 0000 0000 0000 0000 0000
28 0000 0000 0000 0000 0000 0000 0000 0000
29 0000 0000 0000 0000 0000 0000 0000 0000
30 0000 0000 0000 0000 0000 0000 0000 0000
31 0000 0000 0000 0000 0000 0000 0000 0000

32 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
33 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
34 0000 0000 0000 0000 0000 0000 0000 0000
35 0000 0000 0000 0000 0000 0000 0000 0000
36 0000 0000 0000 0000 0000 0000 0000 0000
37 0000 0000 0000 0000 0000 0000 0000 0000
38 0000 0000 0000 0000 0000 0000 0000 0000
39 0000 0000 0000 0000 0000 0000 0000 0000

40 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
41 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
42 0000 0000 0000 0000 0000 0000 0000 0000
43 0000 0000 0000 0000 0000 0000 0000 0000
44 0000 0000 0000 0000 0000 0000 0000 0000
45 0000 0000 0000 0000 0000 0000 0000 0000
46 0000 0000 0000 0000 0000 0000 0000 0000
47 0000 0000 0000 0000 0000 0000 0000 0000

48 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
49 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
50 0000 0000 0000 0000 0000 0000 0000 0000
51 0000 0000 0000 0000 0000 0000 0000 0000
52 0000 0000 0000 0000 0000 0000 0000 0000
53 0000 0000 0000 0000 0000 0000 0000 0000
54 0000 0000 0000 0000 0000 0000 0000 0000
55 0000 0000 0000 0000 0000 0000 0000 0000

56 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
57 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
58 0000 0000 0000 0000 0000 0000 0000 0000
59 0000 0000 0000 0000 0000 0000 0000 0000
60 0000 0000 0000 0000 0000 0000 0000 0000
61 0000 0000 0000 0000 0000 0000 0000 0000
62 0000 0000 0000 0000 0000 0000 0000 0000
63 0000 0000 0000 0000 0000 0000 0000 0000
```

PAL12H6

```
                    11 1111 1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0 0000 0000 0000 0000 0000 0000 0000 0000
 1 0000 0000 0000 0000 0000 0000 0000 0000
 2 0000 0000 0000 0000 0000 0000 0000 0000
 3 0000 0000 0000 0000 0000 0000 0000 0000
 4 0000 0000 0000 0000 0000 0000 0000 0000
 5 0000 0000 0000 0000 0000 0000 0000 0000
 6 0000 0000 0000 0000 0000 0000 0000 0000
 7 0000 0000 0000 0000 0000 0000 0000 0000

 8 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
 9 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
10 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
11 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
12 0000 0000 0000 0000 0000 0000 0000 0000
13 0000 0000 0000 0000 0000 0000 0000 0000
14 0000 0000 0000 0000 0000 0000 0000 0000
15 0000 0000 0000 0000 0000 0000 0000 0000

16 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
17 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
18 0000 0000 0000 0000 0000 0000 0000 0000
19 0000 0000 0000 0000 0000 0000 0000 0000
20 0000 0000 0000 0000 0000 0000 0000 0000
21 0000 0000 0000 0000 0000 0000 0000 0000
22 0000 0000 0000 0000 0000 0000 0000 0000
23 0000 0000 0000 0000 0000 0000 0000 0000

24 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
25 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
26 0000 0000 0000 0000 0000 0000 0000 0000
27 0000 0000 0000 0000 0000 0000 0000 0000
28 0000 0000 0000 0000 0000 0000 0000 0000
29 0000 0000 0000 0000 0000 0000 0000 0000
30 0000 0000 0000 0000 0000 0000 0000 0000
31 0000 0000 0000 0000 0000 0000 0000 0000

32 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
33 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
34 0000 0000 0000 0000 0000 0000 0000 0000
35 0000 0000 0000 0000 0000 0000 0000 0000
36 0000 0000 0000 0000 0000 0000 0000 0000
37 0000 0000 0000 0000 0000 0000 0000 0000
38 0000 0000 0000 0000 0000 0000 0000 0000
39 0000 0000 0000 0000 0000 0000 0000 0000

40 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
41 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
42 0000 0000 0000 0000 0000 0000 0000 0000
43 0000 0000 0000 0000 0000 0000 0000 0000
44 0000 0000 0000 0000 0000 0000 0000 0000
45 0000 0000 0000 0000 0000 0000 0000 0000
46 0000 0000 0000 0000 0000 0000 0000 0000
47 0000 0000 0000 0000 0000 0000 0000 0000

48 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
49 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
50 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
51 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
52 0000 0000 0000 0000 0000 0000 0000 0000
53 0000 0000 0000 0000 0000 0000 0000 0000
54 0000 0000 0000 0000 0000 0000 0000 0000
55 0000 0000 0000 0000 0000 0000 0000 0000

56 0000 0000 0000 0000 0000 0000 0000 0000
57 0000 0000 0000 0000 0000 0000 0000 0000
58 0000 0000 0000 0000 0000 0000 0000 0000
59 0000 0000 0000 0000 0000 0000 0000 0000
60 0000 0000 0000 0000 0000 0000 0000 0000
61 0000 0000 0000 0000 0000 0000 0000 0000
62 0000 0000 0000 0000 0000 0000 0000 0000
63 0000 0000 0000 0000 0000 0000 0000 0000
```

LEGEND: X : FUSE NOT BLOWN (L,N,0) - : FUSE BLOWN (H,P,1)
0 : PHANTOM FUSE (L,N,0) O : PHANTOM FUSE (H,P,1)

PROM Programmer Virgin Fuse Patterns

PAL14H4

```
                    11 1111 1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0 0000 0000 0000 0000 0000 0000 0000 0000
 1 0000 0000 0000 0000 0000 0000 0000 0000
 2 0000 0000 0000 0000 0000 0000 0000 0000
 3 0000 0000 0000 0000 0000 0000 0000 0000
 4 0000 0000 0000 0000 0000 0000 0000 0000
 5 0000 0000 0000 0000 0000 0000 0000 0000
 6 0000 0000 0000 0000 0000 0000 0000 0000
 7 0000 0000 0000 0000 0000 0000 0000 0000

 8 0000 0000 0000 0000 0000 0000 0000 0000
 9 0000 0000 0000 0000 0000 0000 0000 0000
10 0000 0000 0000 0000 0000 0000 0000 0000
11 0000 0000 0000 0000 0000 0000 0000 0000
12 0000 0000 0000 0000 0000 0000 0000 0000
13 0000 0000 0000 0000 0000 0000 0000 0000
14 0000 0000 0000 0000 0000 0000 0000 0000
15 0000 0000 0000 0000 0000 0000 0000 0000

16 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
17 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
18 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
19 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
20 0000 0000 0000 0000 0000 0000 0000 0000
21 0000 0000 0000 0000 0000 0000 0000 0000
22 0000 0000 0000 0000 0000 0000 0000 0000
23 0000 0000 0000 0000 0000 0000 0000 0000

24 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
25 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
26 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
27 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
28 0000 0000 0000 0000 0000 0000 0000 0000
29 0000 0000 0000 0000 0000 0000 0000 0000
30 0000 0000 0000 0000 0000 0000 0000 0000
31 0000 0000 0000 0000 0000 0000 0000 0000

32 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
33 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
34 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
35 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
36 0000 0000 0000 0000 0000 0000 0000 0000
37 0000 0000 0000 0000 0000 0000 0000 0000
38 0000 0000 0000 0000 0000 0000 0000 0000
39 0000 0000 0000 0000 0000 0000 0000 0000

40 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
41 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
42 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
43 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
44 0000 0000 0000 0000 0000 0000 0000 0000
45 0000 0000 0000 0000 0000 0000 0000 0000
46 0000 0000 0000 0000 0000 0000 0000 0000
47 0000 0000 0000 0000 0000 0000 0000 0000

48 0000 0000 0000 0000 0000 0000 0000 0000
49 0000 0000 0000 0000 0000 0000 0000 0000
50 0000 0000 0000 0000 0000 0000 0000 0000
51 0000 0000 0000 0000 0000 0000 0000 0000
52 0000 0000 0000 0000 0000 0000 0000 0000
53 0000 0000 0000 0000 0000 0000 0000 0000
54 0000 0000 0000 0000 0000 0000 0000 0000
55 0000 0000 0000 0000 0000 0000 0000 0000

56 0000 0000 0000 0000 0000 0000 0000 0000
57 0000 0000 0000 0000 0000 0000 0000 0000
58 0000 0000 0000 0000 0000 0000 0000 0000
59 0000 0000 0000 0000 0000 0000 0000 0000
60 0000 0000 0000 0000 0000 0000 0000 0000
61 0000 0000 0000 0000 0000 0000 0000 0000
62 0000 0000 0000 0000 0000 0000 0000 0000
63 0000 0000 0000 0000 0000 0000 0000 0000
```

PAL16H2

```
                    11 1111 1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0 0000 0000 0000 0000 0000 0000 0000 0000
 1 0000 0000 0000 0000 0000 0000 0000 0000
 2 0000 0000 0000 0000 0000 0000 0000 0000
 3 0000 0000 0000 0000 0000 0000 0000 0000
 4 0000 0000 0000 0000 0000 0000 0000 0000
 5 0000 0000 0000 0000 0000 0000 0000 0000
 6 0000 0000 0000 0000 0000 0000 0000 0000
 7 0000 0000 0000 0000 0000 0000 0000 0000

 8 0000 0000 0000 0000 0000 0000 0000 0000
 9 0000 0000 0000 0000 0000 0000 0000 0000
10 0000 0000 0000 0000 0000 0000 0000 0000
11 0000 0000 0000 0000 0000 0000 0000 0000
12 0000 0000 0000 0000 0000 0000 0000 0000
13 0000 0000 0000 0000 0000 0000 0000 0000
14 0000 0000 0000 0000 0000 0000 0000 0000
15 0000 0000 0000 0000 0000 0000 0000 0000

16 0000 0000 0000 0000 0000 0000 0000 0000
17 0000 0000 0000 0000 0000 0000 0000 0000
18 0000 0000 0000 0000 0000 0000 0000 0000
19 0000 0000 0000 0000 0000 0000 0000 0000
20 0000 0000 0000 0000 0000 0000 0000 0000
21 0000 0000 0000 0000 0000 0000 0000 0000
22 0000 0000 0000 0000 0000 0000 0000 0000
23 0000 0000 0000 0000 0000 0000 0000 0000

24 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
25 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
26 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
27 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
28 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
29 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
30 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
31 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

32 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
33 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
34 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
35 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
36 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
37 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
38 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
39 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

40 0000 0000 0000 0000 0000 0000 0000 0000
41 0000 0000 0000 0000 0000 0000 0000 0000
42 0000 0000 0000 0000 0000 0000 0000 0000
43 0000 0000 0000 0000 0000 0000 0000 0000
44 0000 0000 0000 0000 0000 0000 0000 0000
45 0000 0000 0000 0000 0000 0000 0000 0000
46 0000 0000 0000 0000 0000 0000 0000 0000
47 0000 0000 0000 0000 0000 0000 0000 0000

48 0000 0000 0000 0000 0000 0000 0000 0000
49 0000 0000 0000 0000 0000 0000 0000 0000
50 0000 0000 0000 0000 0000 0000 0000 0000
51 0000 0000 0000 0000 0000 0000 0000 0000
52 0000 0000 0000 0000 0000 0000 0000 0000
53 0000 0000 0000 0000 0000 0000 0000 0000
54 0000 0000 0000 0000 0000 0000 0000 0000
55 0000 0000 0000 0000 0000 0000 0000 0000

56 0000 0000 0000 0000 0000 0000 0000 0000
57 0000 0000 0000 0000 0000 0000 0000 0000
58 0000 0000 0000 0000 0000 0000 0000 0000
59 0000 0000 0000 0000 0000 0000 0000 0000
60 0000 0000 0000 0000 0000 0000 0000 0000
61 0000 0000 0000 0000 0000 0000 0000 0000
62 0000 0000 0000 0000 0000 0000 0000 0000
63 0000 0000 0000 0000 0000 0000 0000 0000
```

LEGEND: X : FUSE NOT BLOWN (L,N,0) - : FUSE BLOWN (H,P,1)
0 : PHANTOM FUSE (L,N,0) O : PHANTOM FUSE (H,P,1)

PROM Programmer Virgin Fuse Patterns

PAL10L8

```
                    11 1111 1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
 1 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
 2 0000 0000 0000 0000 0000 0000 0000 0000
 3 0000 0000 0000 0000 0000 0000 0000 0000
 4 0000 0000 0000 0000 0000 0000 0000 0000
 5 0000 0000 0000 0000 0000 0000 0000 0000
 6 0000 0000 0000 0000 0000 0000 0000 0000
 7 0000 0000 0000 0000 0000 0000 0000 0000

 8 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
 9 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
10 0000 0000 0000 0000 0000 0000 0000 0000
11 0000 0000 0000 0000 0000 0000 0000 0000
12 0000 0000 0000 0000 0000 0000 0000 0000
13 0000 0000 0000 0000 0000 0000 0000 0000
14 0000 0000 0000 0000 0000 0000 0000 0000
15 0000 0000 0000 0000 0000 0000 0000 0000

16 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
17 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
18 0000 0000 0000 0000 0000 0000 0000 0000
19 0000 0000 0000 0000 0000 0000 0000 0000
20 0000 0000 0000 0000 0000 0000 0000 0000
21 0000 0000 0000 0000 0000 0000 0000 0000
22 0000 0000 0000 0000 0000 0000 0000 0000
23 0000 0000 0000 0000 0000 0000 0000 0000

24 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
25 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
26 0000 0000 0000 0000 0000 0000 0000 0000
27 0000 0000 0000 0000 0000 0000 0000 0000
28 0000 0000 0000 0000 0000 0000 0000 0000
29 0000 0000 0000 0000 0000 0000 0000 0000
30 0000 0000 0000 0000 0000 0000 0000 0000
31 0000 0000 0000 0000 0000 0000 0000 0000

32 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
33 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
34 0000 0000 0000 0000 0000 0000 0000 0000
35 0000 0000 0000 0000 0000 0000 0000 0000
36 0000 0000 0000 0000 0000 0000 0000 0000
37 0000 0000 0000 0000 0000 0000 0000 0000
38 0000 0000 0000 0000 0000 0000 0000 0000
39 0000 0000 0000 0000 0000 0000 0000 0000

40 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
41 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
42 0000 0000 0000 0000 0000 0000 0000 0000
43 0000 0000 0000 0000 0000 0000 0000 0000
44 0000 0000 0000 0000 0000 0000 0000 0000
45 0000 0000 0000 0000 0000 0000 0000 0000
46 0000 0000 0000 0000 0000 0000 0000 0000
47 0000 0000 0000 0000 0000 0000 0000 0000

48 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
49 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
50 0000 0000 0000 0000 0000 0000 0000 0000
51 0000 0000 0000 0000 0000 0000 0000 0000
52 0000 0000 0000 0000 0000 0000 0000 0000
53 0000 0000 0000 0000 0000 0000 0000 0000
54 0000 0000 0000 0000 0000 0000 0000 0000
55 0000 0000 0000 0000 0000 0000 0000 0000

56 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
57 XXXX XXOO XXOO XXOO XXOO XXOO XXOO XXXX
58 0000 0000 0000 0000 0000 0000 0000 0000
59 0000 0000 0000 0000 0000 0000 0000 0000
60 0000 0000 0000 0000 0000 0000 0000 0000
61 0000 0000 0000 0000 0000 0000 0000 0000
62 0000 0000 0000 0000 0000 0000 0000 0000
63 0000 0000 0000 0000 0000 0000 0000 0000
```

PAL12L6

```
                    11 1111 1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0 0000 0000 0000 0000 0000 0000 0000 0000
 1 0000 0000 0000 0000 0000 0000 0000 0000
 2 0000 0000 0000 0000 0000 0000 0000 0000
 3 0000 0000 0000 0000 0000 0000 0000 0000
 4 0000 0000 0000 0000 0000 0000 0000 0000
 5 0000 0000 0000 0000 0000 0000 0000 0000
 6 0000 0000 0000 0000 0000 0000 0000 0000
 7 0000 0000 0000 0000 0000 0000 0000 0000

 8 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
 9 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
10 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
11 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
12 0000 0000 0000 0000 0000 0000 0000 0000
13 0000 0000 0000 0000 0000 0000 0000 0000
14 0000 0000 0000 0000 0000 0000 0000 0000
15 0000 0000 0000 0000 0000 0000 0000 0000

16 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
17 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
18 0000 0000 0000 0000 0000 0000 0000 0000
19 0000 0000 0000 0000 0000 0000 0000 0000
20 0000 0000 0000 0000 0000 0000 0000 0000
21 0000 0000 0000 0000 0000 0000 0000 0000
22 0000 0000 0000 0000 0000 0000 0000 0000
23 0000 0000 0000 0000 0000 0000 0000 0000

24 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
25 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
26 0000 0000 0000 0000 0000 0000 0000 0000
27 0000 0000 0000 0000 0000 0000 0000 0000
28 0000 0000 0000 0000 0000 0000 0000 0000
29 0000 0000 0000 0000 0000 0000 0000 0000
30 0000 0000 0000 0000 0000 0000 0000 0000
31 0000 0000 0000 0000 0000 0000 0000 0000

32 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
33 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
34 0000 0000 0000 0000 0000 0000 0000 0000
35 0000 0000 0000 0000 0000 0000 0000 0000
36 0000 0000 0000 0000 0000 0000 0000 0000
37 0000 0000 0000 0000 0000 0000 0000 0000
38 0000 0000 0000 0000 0000 0000 0000 0000
39 0000 0000 0000 0000 0000 0000 0000 0000

40 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
41 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
42 0000 0000 0000 0000 0000 0000 0000 0000
43 0000 0000 0000 0000 0000 0000 0000 0000
44 0000 0000 0000 0000 0000 0000 0000 0000
45 0000 0000 0000 0000 0000 0000 0000 0000
46 0000 0000 0000 0000 0000 0000 0000 0000
47 0000 0000 0000 0000 0000 0000 0000 0000

48 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
49 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
50 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
51 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
52 0000 0000 0000 0000 0000 0000 0000 0000
53 0000 0000 0000 0000 0000 0000 0000 0000
54 0000 0000 0000 0000 0000 0000 0000 0000
55 0000 0000 0000 0000 0000 0000 0000 0000

56 0000 0000 0000 0000 0000 0000 0000 0000
57 0000 0000 0000 0000 0000 0000 0000 0000
58 0000 0000 0000 0000 0000 0000 0000 0000
59 0000 0000 0000 0000 0000 0000 0000 0000
60 0000 0000 0000 0000 0000 0000 0000 0000
61 0000 0000 0000 0000 0000 0000 0000 0000
62 0000 0000 0000 0000 0000 0000 0000 0000
63 0000 0000 0000 0000 0000 0000 0000 0000
```

LEGEND: X : FUSE NOT BLOWN (L,N,0) - : FUSE BLOWN (H,P,1)
0 : PHANTOM FUSE (L,N,0) O : PHANTOM FUSE (H,P,1)

PROM Programmer Virgin Fuse Patterns

PAL14L4

```
                    11 1111 1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0 0000 0000 0000 0000 0000 0000 0000 0000
 1 0000 0000 0000 0000 0000 0000 0000 0000
 2 0000 0000 0000 0000 0000 0000 0000 0000
 3 0000 0000 0000 0000 0000 0000 0000 0000
 4 0000 0000 0000 0000 0000 0000 0000 0000
 5 0000 0000 0000 0000 0000 0000 0000 0000
 6 0000 0000 0000 0000 0000 0000 0000 0000
 7 0000 0000 0000 0000 0000 0000 0000 0000

 8 0000 0000 0000 0000 0000 0000 0000 0000
 9 0000 0000 0000 0000 0000 0000 0000 0000
10 0000 0000 0000 0000 0000 0000 0000 0000
11 0000 0000 0000 0000 0000 0000 0000 0000
12 0000 0000 0000 0000 0000 0000 0000 0000
13 0000 0000 0000 0000 0000 0000 0000 0000
14 0000 0000 0000 0000 0000 0000 0000 0000
15 0000 0000 0000 0000 0000 0000 0000 0000

16 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
17 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
18 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
19 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
20 0000 0000 0000 0000 0000 0000 0000 0000
21 0000 0000 0000 0000 0000 0000 0000 0000
22 0000 0000 0000 0000 0000 0000 0000 0000
23 0000 0000 0000 0000 0000 0000 0000 0000

24 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
25 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
26 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
27 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
28 0000 0000 0000 0000 0000 0000 0000 0000
29 0000 0000 0000 0000 0000 0000 0000 0000
30 0000 0000 0000 0000 0000 0000 0000 0000
31 0000 0000 0000 0000 0000 0000 0000 0000

32 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
33 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
34 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
35 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
36 0000 0000 0000 0000 0000 0000 0000 0000
37 0000 0000 0000 0000 0000 0000 0000 0000
38 0000 0000 0000 0000 0000 0000 0000 0000
39 0000 0000 0000 0000 0000 0000 0000 0000

40 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
41 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
42 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
43 XXXX XXXX XXXX XXOO XXOO XXXX XXXX XXXX
44 0000 0000 0000 0000 0000 0000 0000 0000
45 0000 0000 0000 0000 0000 0000 0000 0000
46 0000 0000 0000 0000 0000 0000 0000 0000
47 0000 0000 0000 0000 0000 0000 0000 0000

48 0000 0000 0000 0000 0000 0000 0000 0000
49 0000 0000 0000 0000 0000 0000 0000 0000
50 0000 0000 0000 0000 0000 0000 0000 0000
51 0000 0000 0000 0000 0000 0000 0000 0000
52 0000 0000 0000 0000 0000 0000 0000 0000
53 0000 0000 0000 0000 0000 0000 0000 0000
54 0000 0000 0000 0000 0000 0000 0000 0000
55 0000 0000 0000 0000 0000 0000 0000 0000

56 0000 0000 0000 0000 0000 0000 0000 0000
57 0000 0000 0000 0000 0000 0000 0000 0000
58 0000 0000 0000 0000 0000 0000 0000 0000
59 0000 0000 0000 0000 0000 0000 0000 0000
60 0000 0000 0000 0000 0000 0000 0000 0000
61 0000 0000 0000 0000 0000 0000 0000 0000
62 0000 0000 0000 0000 0000 0000 0000 0000
63 0000 0000 0000 0000 0000 0000 0000 0000
```

LEGEND: X : FUSE NOT BLOWN (L,N,0)
0 : PHANTOM FUSE (L,N,0)

PAL16L2

```
                    11 1111 1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0 0000 0000 0000 0000 0000 0000 0000 0000
 1 0000 0000 0000 0000 0000 0000 0000 0000
 2 0000 0000 0000 0000 0000 0000 0000 0000
 3 0000 0000 0000 0000 0000 0000 0000 0000
 4 0000 0000 0000 0000 0000 0000 0000 0000
 5 0000 0000 0000 0000 0000 0000 0000 0000
 6 0000 0000 0000 0000 0000 0000 0000 0000
 7 0000 0000 0000 0000 0000 0000 0000 0000

 8 0000 0000 0000 0000 0000 0000 0000 0000
 9 0000 0000 0000 0000 0000 0000 0000 0000
10 0000 0000 0000 0000 0000 0000 0000 0000
11 0000 0000 0000 0000 0000 0000 0000 0000
12 0000 0000 0000 0000 0000 0000 0000 0000
13 0000 0000 0000 0000 0000 0000 0000 0000
14 0000 0000 0000 0000 0000 0000 0000 0000
15 0000 0000 0000 0000 0000 0000 0000 0000

16 0000 0000 0000 0000 0000 0000 0000 0000
17 0000 0000 0000 0000 0000 0000 0000 0000
18 0000 0000 0000 0000 0000 0000 0000 0000
19 0000 0000 0000 0000 0000 0000 0000 0000
20 0000 0000 0000 0000 0000 0000 0000 0000
21 0000 0000 0000 0000 0000 0000 0000 0000
22 0000 0000 0000 0000 0000 0000 0000 0000
23 0000 0000 0000 0000 0000 0000 0000 0000

24 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
25 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
26 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
27 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
28 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
29 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
30 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
31 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

32 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
33 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
34 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
35 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
36 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
37 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
38 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
39 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

40 0000 0000 0000 0000 0000 0000 0000 0000
41 0000 0000 0000 0000 0000 0000 0000 0000
42 0000 0000 0000 0000 0000 0000 0000 0000
43 0000 0000 0000 0000 0000 0000 0000 0000
44 0000 0000 0000 0000 0000 0000 0000 0000
45 0000 0000 0000 0000 0000 0000 0000 0000
46 0000 0000 0000 0000 0000 0000 0000 0000
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48 0000 0000 0000 0000 0000 0000 0000 0000
49 0000 0000 0000 0000 0000 0000 0000 0000
50 0000 0000 0000 0000 0000 0000 0000 0000
51 0000 0000 0000 0000 0000 0000 0000 0000
52 0000 0000 0000 0000 0000 0000 0000 0000
53 0000 0000 0000 0000 0000 0000 0000 0000
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56 0000 0000 0000 0000 0000 0000 0000 0000
57 0000 0000 0000 0000 0000 0000 0000 0000
58 0000 0000 0000 0000 0000 0000 0000 0000
59 0000 0000 0000 0000 0000 0000 0000 0000
60 0000 0000 0000 0000 0000 0000 0000 0000
61 0000 0000 0000 0000 0000 0000 0000 0000
62 0000 0000 0000 0000 0000 0000 0000 0000
63 0000 0000 0000 0000 0000 0000 0000 0000
```

- : FUSE BLOWN (H,P,1)
O : PHANTOM FUSE (H,P,1)

PROM Programmer Virgin Fuse Patterns

PAL16C1

```
                    11 1111 1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0 0000 0000 0000 0000 0000 0000 0000 0000
 1 0000 0000 0000 0000 0000 0000 0000 0000
 2 0000 0000 0000 0000 0000 0000 0000 0000
 3 0000 0000 0000 0000 0000 0000 0000 0000
 4 0000 0000 0000 0000 0000 0000 0000 0000
 5 0000 0000 0000 0000 0000 0000 0000 0000
 6 0000 0000 0000 0000 0000 0000 0000 0000
 7 0000 0000 0000 0000 0000 0000 0000 0000

 8 0000 0000 0000 0000 0000 0000 0000 0000
 9 0000 0000 0000 0000 0000 0000 0000 0000
10 0000 0000 0000 0000 0000 0000 0000 0000
11 0000 0000 0000 0000 0000 0000 0000 0000
12 0000 0000 0000 0000 0000 0000 0000 0000
13 0000 0000 0000 0000 0000 0000 0000 0000
14 0000 0000 0000 0000 0000 0000 0000 0000
15 0000 0000 0000 0000 0000 0000 0000 0000

16 0000 0000 0000 0000 0000 0000 0000 0000
17 0000 0000 0000 0000 0000 0000 0000 0000
18 0000 0000 0000 0000 0000 0000 0000 0000
19 0000 0000 0000 0000 0000 0000 0000 0000
20 0000 0000 0000 0000 0000 0000 0000 0000
21 0000 0000 0000 0000 0000 0000 0000 0000
22 0000 0000 0000 0000 0000 0000 0000 0000
23 0000 0000 0000 0000 0000 0000 0000 0000

24 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
25 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
26 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
27 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
28 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
29 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
30 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
31 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

32 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
33 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
34 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
35 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
36 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
37 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
38 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
39 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

40 0000 0000 0000 0000 0000 0000 0000 0000
41 0000 0000 0000 0000 0000 0000 0000 0000
42 0000 0000 0000 0000 0000 0000 0000 0000
43 0000 0000 0000 0000 0000 0000 0000 0000
44 0000 0000 0000 0000 0000 0000 0000 0000
45 0000 0000 0000 0000 0000 0000 0000 0000
46 0000 0000 0000 0000 0000 0000 0000 0000
47 0000 0000 0000 0000 0000 0000 0000 0000

48 0000 0000 0000 0000 0000 0000 0000 0000
49 0000 0000 0000 0000 0000 0000 0000 0000
50 0000 0000 0000 0000 0000 0000 0000 0000
51 0000 0000 0000 0000 0000 0000 0000 0000
52 0000 0000 0000 0000 0000 0000 0000 0000
53 0000 0000 0000 0000 0000 0000 0000 0000
54 0000 0000 0000 0000 0000 0000 0000 0000
55 0000 0000 0000 0000 0000 0000 0000 0000

56 0000 0000 0000 0000 0000 0000 0000 0000
57 0000 0000 0000 0000 0000 0000 0000 0000
58 0000 0000 0000 0000 0000 0000 0000 0000
59 0000 0000 0000 0000 0000 0000 0000 0000
60 0000 0000 0000 0000 0000 0000 0000 0000
61 0000 0000 0000 0000 0000 0000 0000 0000
62 0000 0000 0000 0000 0000 0000 0000 0000
63 0000 0000 0000 0000 0000 0000 0000 0000
```

PAL16L8, 16R8, 16R6, 16R4

```
                    11 1111 1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 1 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 2 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 3 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 4 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 5 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 6 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 7 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

 8 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 9 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
10 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
11 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
12 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
13 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
14 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
15 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

16 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
17 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
18 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
19 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
20 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
21 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
22 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
23 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

24 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
25 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
26 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
27 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
28 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
29 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
30 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
31 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

32 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
33 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
34 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
35 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
36 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
37 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
38 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
39 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

40 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
41 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
42 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
43 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
44 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
45 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
46 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
47 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

48 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
49 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
50 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
51 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
52 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
53 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
54 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
55 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

56 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
57 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
58 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
59 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
60 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
61 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
62 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
63 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
```

LEGEND: X : FUSE NOT BLOWN (L,N,0) - : FUSE BLOWN (H,P,1)
0 : PHANTOM FUSE (L,N,0) O : PHANTOM FUSE (H,P,1)

MANUAL CODING

Logic Diagrams

The phantom fuse locations are shown on pages 6-48 thru 6-65. Note that the input and product terms that were missing in the logic diagrams of previous section on pages 6-14 thru 6-22 are now being shown as phantom fuse locations. These locations are filled in according to the Table 1 on page 6-30.

The remaining locations are the nodes where fuses are intact. Fuses left intact are indicated by an "X" at the intersection of the input line and the product term. A blown fuse is not marked. The PAL logic diagrams are provided with no fuses marked, allowing a designer to put an "X" on the nodes where a fuse is to remain intact and leave the other nodes blank.

Once the logic diagram is completed, this information must be transferred to the programming format. Each fuse node is identified by a product line number and an input line number which are used to locate the corresponding square in the PAL programming format.

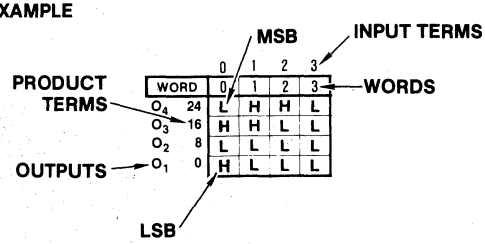
The following legend is being used:

Logic Diagram	Programming format
	L, N, O
	H, P, 1
	Phantom Fuse Location (H, P, 1)
	Phantom Fuse Location (L, N, O)

Programming Format:

The programming format is designed such that it is compatible with standard PROM programmer format for 512x4 (2048-bit) PROM. Words addresses are in HEX since most of the PROM programmers use HEX addresses. A table which contains HEX to decimal conversion is also provided on page 6-75. Referring to page 6-49 note that the input lines go from left to right and are in sequence. The product terms go from top to bottom and are not in sequence and are scrambled. This is because, to form one 4-bit word, we need four different product terms on the same input line. A word is read from top to bottom and consists of four product terms on one input line. The top bit is most significant (MSB) and the bottom bit is least significant (LSB).

EXAMPLE



WORD 0 : LHLH

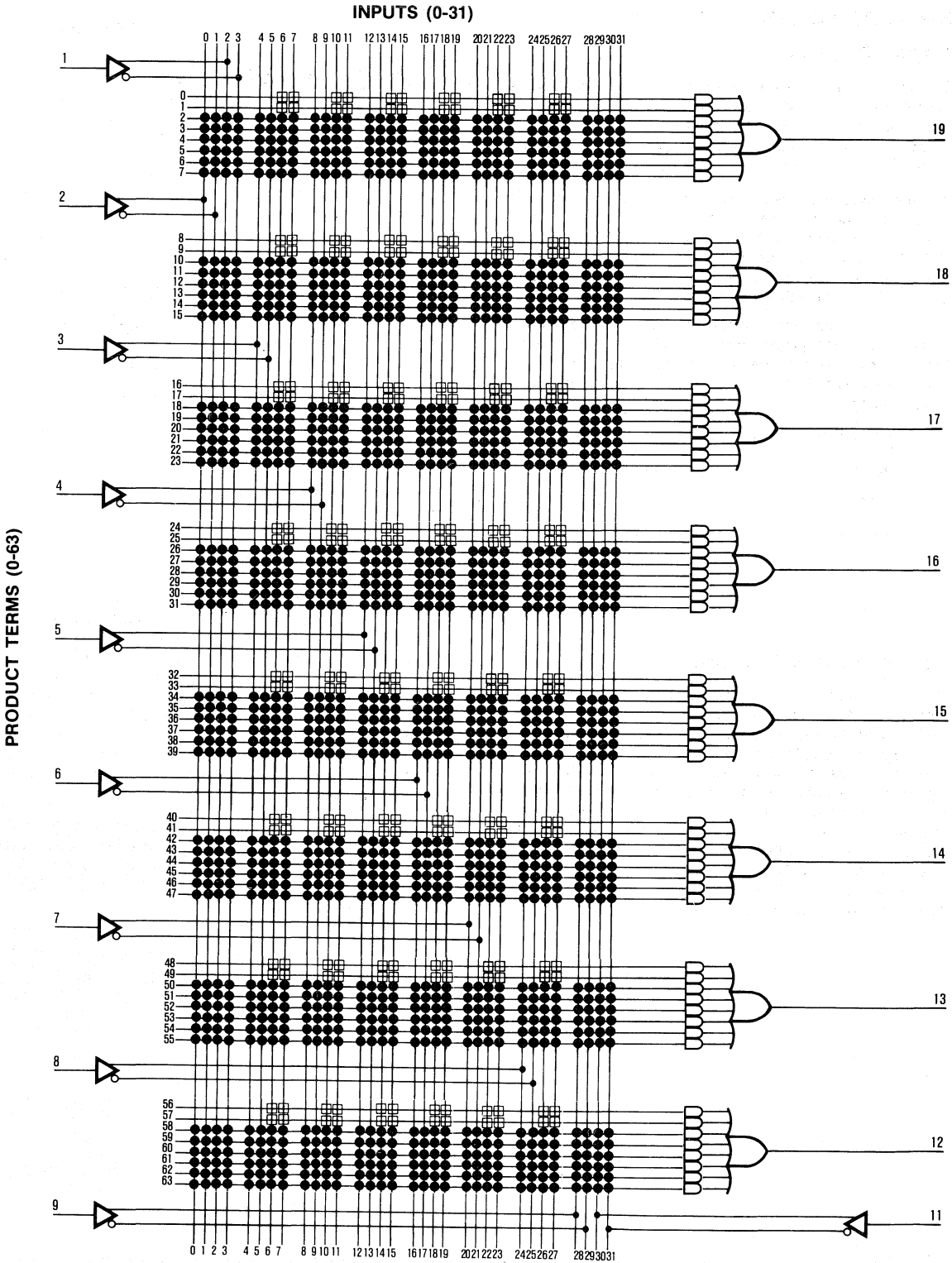
WORD 1 : HHLL

WORD 2 : HLLL

WORD 3 : LLLL

As in the case of logic diagrams, the programming format for the first nine PALs are filled with an 'H' or an 'L' representing the phantom fuse locations. The remaining blank squares are to be filled by the designer. If one decides to use a programming format other than BHLF, then 'H' and 'L' will have to be converted into the equivalent format. (e.g., if one decides to use BPNF format, then 'H' has to be replaced by 'P' and 'L' has to be replaced by 'N' on the programming format). Logic diagrams and the programming formats for all different options are shown on pages 6-48 thru 6-73.

The most common PROM programmer input medium is paper tape, with BHLF, BPNF or HEXADECIMAL format. Information regarding generation of paper tape and different formats are described on page 6-74.



LEGEND: ● : Phantom Fuse (L, N, 0) □ : Phantom Fuse (H, P, 1) n.u. — not used

Programming Format

PAL10H8

PATTERN: _____

NAME: _____

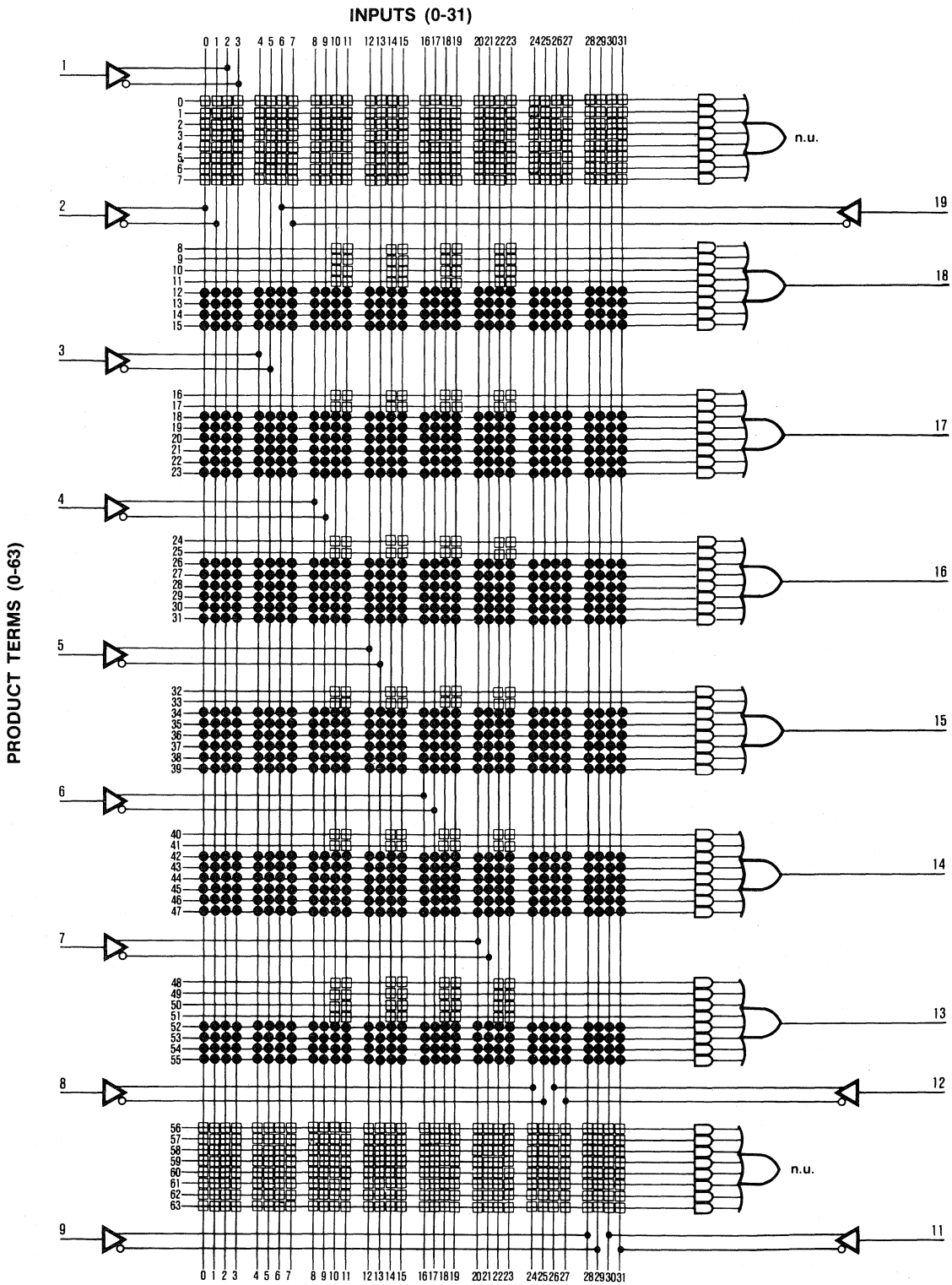
DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24							H	H			H	H			H	H			H	H			H	H			H	H				
O_3 16							H	H			H	H			H	H			H	H			H	H			H	H				
O_2 8							H	H			H	H			H	H			H	H			H	H			H	H				
O_1 0							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25							H	H			H	H			H	H			H	H			H	H			H	H				
O_3 17							H	H			H	H			H	H			H	H			H	H			H	H				
O_2 9							H	H			H	H			H	H			H	H			H	H			H	H				
O_1 1							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 18	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 10	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 2	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 19	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 11	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 3	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 13	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 5	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 14	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 6	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 7	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56							H	H			H	H			H	H			H	H			H	H			H	H				
O_3 48							H	H			H	H			H	H			H	H			H	H			H	H				
O_2 40							H	H			H	H			H	H			H	H			H	H			H	H				
O_1 32							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57							H	H			H	H			H	H			H	H			H	H			H	H				
O_3 49							H	H			H	H			H	H			H	H			H	H			H	H				
O_2 41							H	H			H	H			H	H			H	H			H	H			H	H				
O_1 33							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 50	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 42	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 34	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 51	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 43	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 35	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

6



LEGEND: ● : Phantom Fuse (L, N, 0) □ : Phantom Fuse (H, P, 1) n.u. — not used

PATTERN: _____ NAME: _____

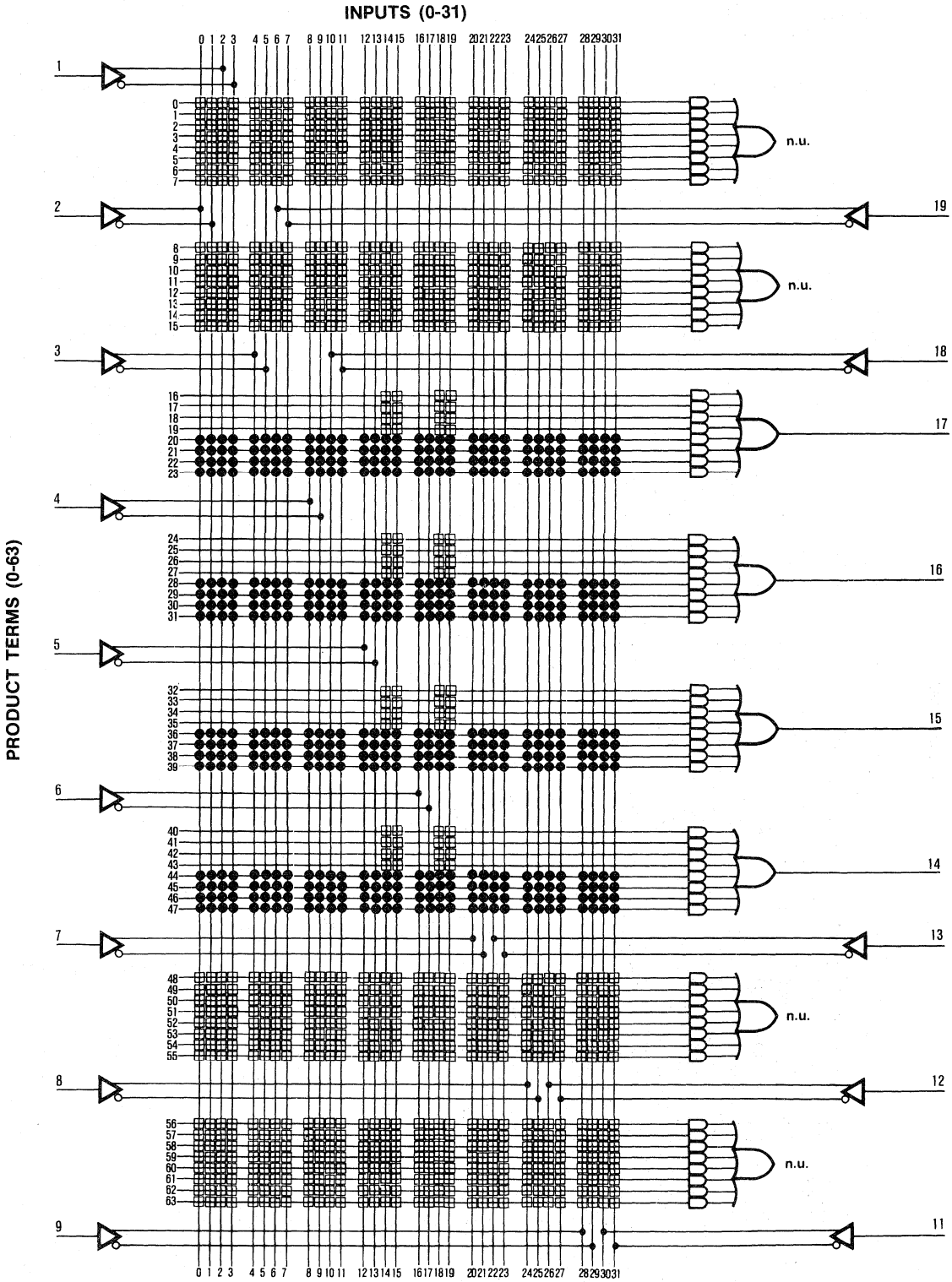
DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24											H	H			H	H			H	H			H	H								
O_3 16											H	H			H	H			H	H			H	H								
O_2 8											H	H			H	H			H	H			H	H								
O_1 0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25											H	H			H	H			H	H			H	H								
O_3 17											H	H			H	H			H	H			H	H								
O_2 9											H	H			H	H			H	H			H	H								
O_1 1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 18	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 10											H	H			H	H			H	H			H	H								
O_1 2	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 19	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 11											H	H							H	H			H	H								
O_1 3	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 4	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 13	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 5	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 14	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 6	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 7	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 48											H	H			H	H			H	H			H	H								
O_2 40											H	H			H	H			H	H			H	H								
O_1 32											H	H			H	H			H	H			H	H								
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 49											H	H			H	H			H	H			H	H								
O_2 41											H	H			H	H			H	H			H	H								
O_1 33											H	H			H	H			H	H			H	H								
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 50											H	H			H	H			H	H			H	H								
O_2 42	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 34	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 51											H	H			H	H			H	H			H	H								
O_2 43	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 35	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

6



LEGEND: ● : Phantom Fuse (L, N, 0) □ : Phantom Fuse (H, P, 1) n.u. — not used

PAL14H4

PATTERN: _____

NAME: _____

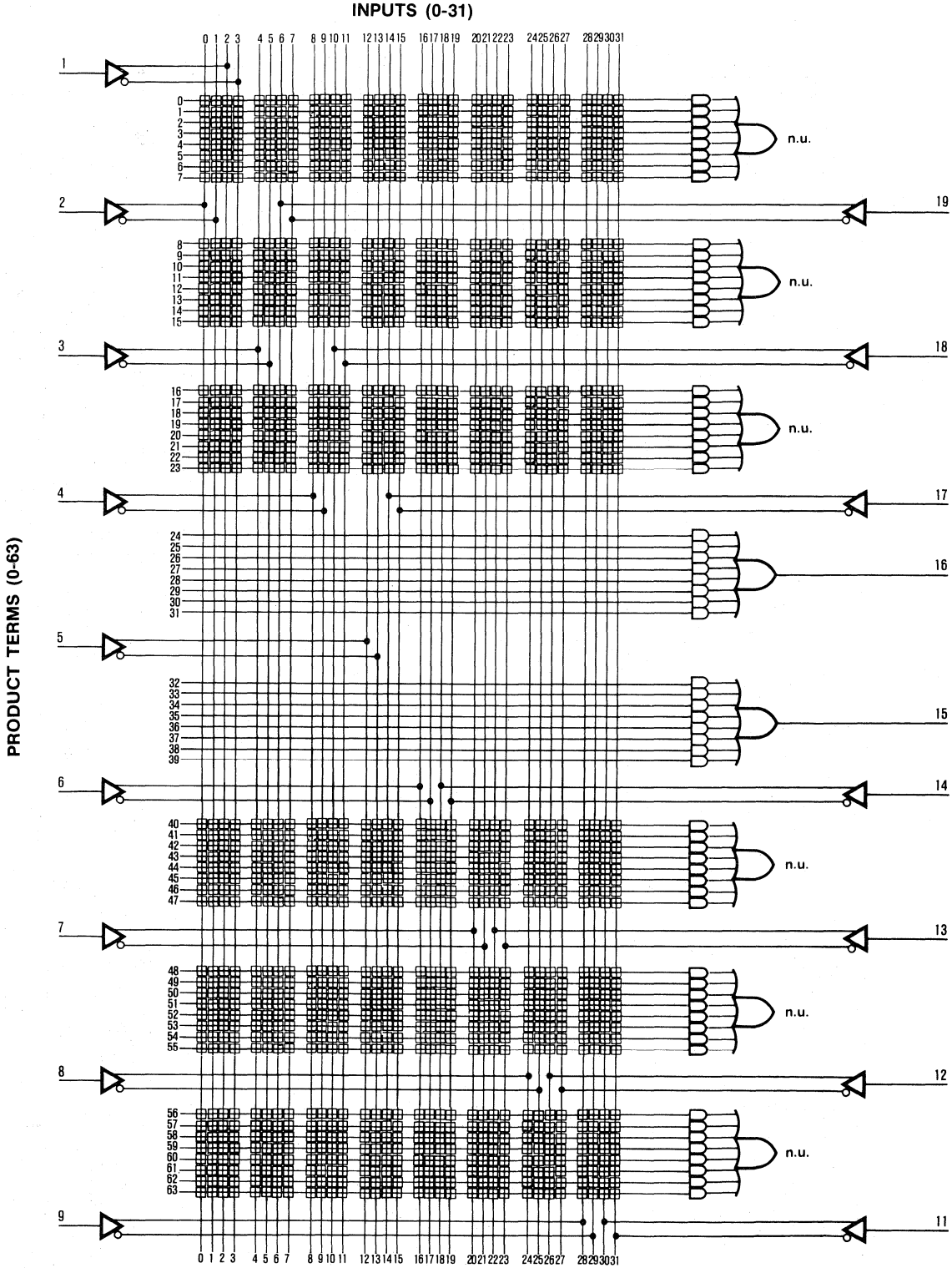
DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24															H	H			H	H												
O_3 16															H	H			H	H												
O_2 8	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25															H	H			H	H												
O_3 17															H	H			H	H												
O_2 9	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26															H	H			H	H												
O_3 18															H	H			H	H												
O_2 10	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 2	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27															H	H			H	H												
O_3 19															H	H			H	H												
O_2 11	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 3	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 12	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 4	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 13	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 5	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 14	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 6	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 15	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 7	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 48	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 40															H	H			H	H												
O_1 32															H	H			H	H												
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 49	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 41															H	H			H	H												
O_1 33															H	H			H	H												
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 50	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 42															H	H			H	H												
O_1 34															H	H			H	H												
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 51	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 43															H	H			H	H												
O_1 35															H	H			H	H												
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 52	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 53	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 54	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 55	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

6



LEGEND: ● : Phantom Fuse (L, N, 0) □ : Phantom Fuse (H, P, 1) n.u. — not used

Programming Format

PAL16H2

PATTERN:

NAME:

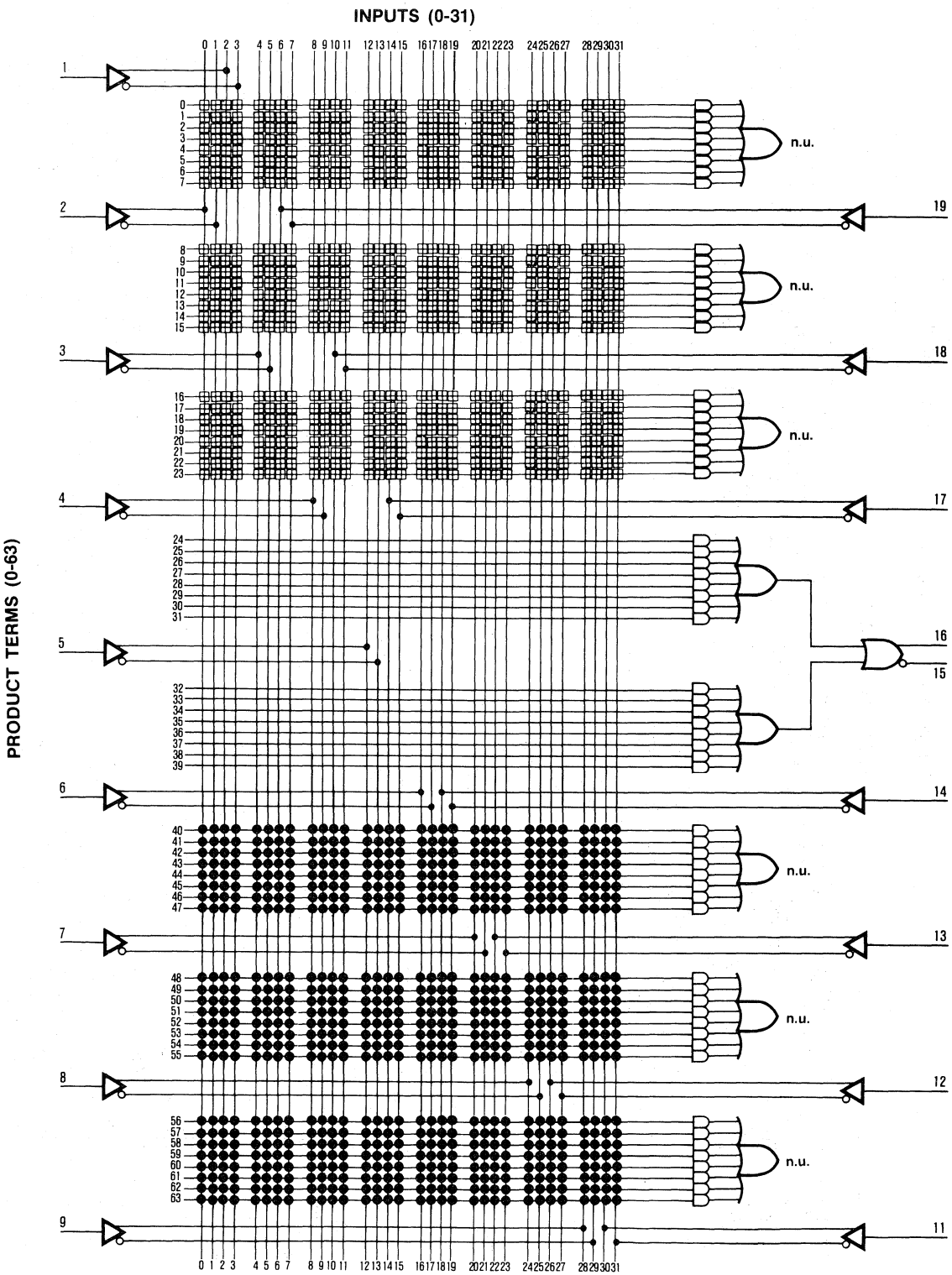
PRODUCT TERMS (0-63)

DATE:

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24																																
O_3 16	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 8	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25																																
O_3 17	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 9	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26																																
O_3 18	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 10	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 2	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27																																
O_3 19	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 11	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 3	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28																																
O_3 20	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 12	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 4	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29																																
O_3 21	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 13	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 5	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30																																
O_3 22	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 14	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 6	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31																																
O_3 23	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 15	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 7	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 48	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 40	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 49	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 41	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 50	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 42	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 51	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 43	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 52	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 44	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 53	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 45	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 54	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 46	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 55	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 47	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

6



LEGEND: ● : Phantom Fuse (L, N, 0) □ : Phantom Fuse (H, P, 1) n.u. — not used

PAL16C1

PATTERN: _____

NAME: _____

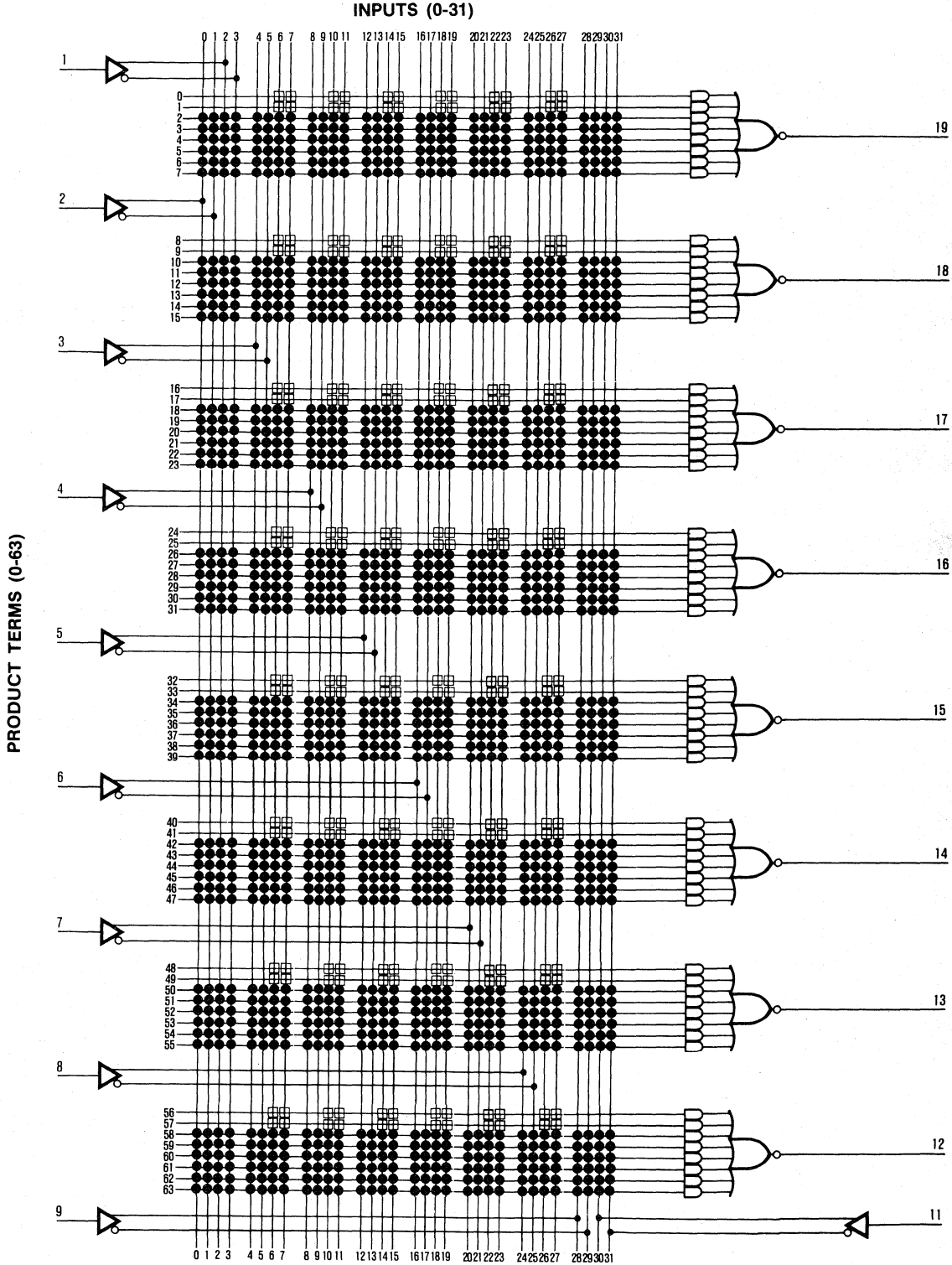
DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24																																
O_3 16	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 8	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25																																
O_3 17	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 9	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26																																
O_3 18	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 10	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 2	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27																																
O_3 19	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 11	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 3	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28																																
O_3 20	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 12	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 4	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29																																
O_3 21	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 13	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 5	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30																																
O_3 22	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 14	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 6	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31																																
O_3 23	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 15	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 7	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 48	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 40	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 49	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 41	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 50	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 42	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 51	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 43	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

6



LEGEND: ● : Phantom Fuse (L, N, 0) □ : Phantom Fuse (H, P, 1) n.u. — not used

PAL10L8

PATTERN: _____

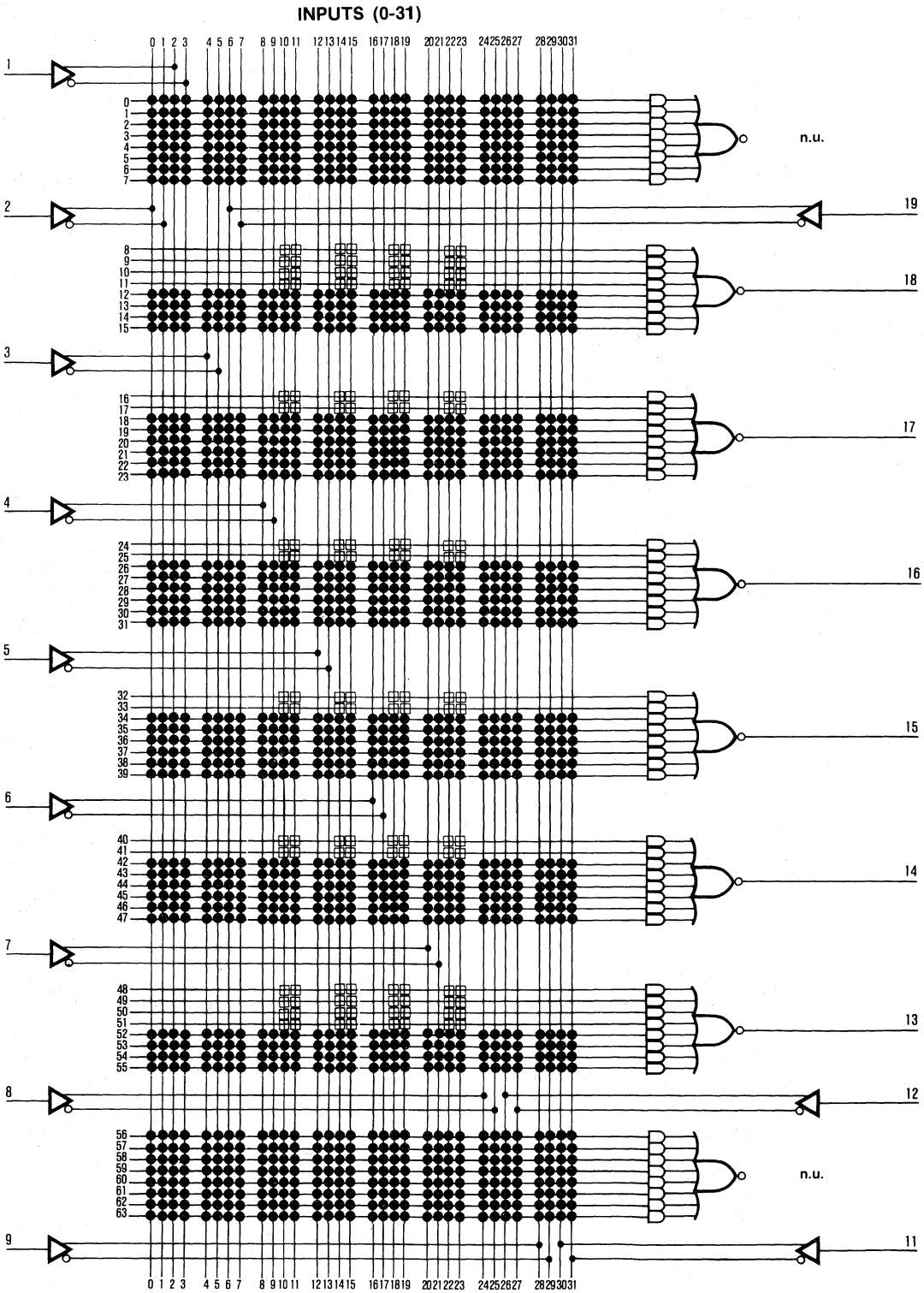
NAME: _____

DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24							H	H			H	H			H	H			H	H			H	H			H	H				
O_3 16							H	H			H	H			H	H			H	H			H	H			H	H				
O_2 8							H	H			H	H			H	H			H	H			H	H			H	H				
O_1 0							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25							H	H			H	H			H	H			H	H			H	H			H	H				
O_3 17							H	H			H	H			H	H			H	H			H	H			H	H				
O_2 9							H	H			H	H			H	H			H	H			H	H			H	H				
O_1 1							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 18	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 10	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 2	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 19	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 11	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 3	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 13	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 5	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 14	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 6	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 7	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56							H	H			H	H			H	H			H	H			H	H			H	H				
O_3 48							H	H			H	H			H	H			H	H			H	H			H	H				
O_2 40							H	H			H	H			H	H			H	H			H	H			H	H				
O_1 32							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57							H	H			H	H			H	H			H	H			H	H			H	H				
O_3 49							H	H			H	H			H	H			H	H			H	H			H	H				
O_2 41							H	H			H	H			H	H			H	H			H	H			H	H				
O_1 33							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 50	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 42	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 34	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 51	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 43	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 35	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31



LEGEND: ● : Phantom Fuse (L, N, 0) □ : Phantom Fuse (H, P, 1) n.u. — not used

Programming Format

PAL12L6

PATTERN:

NAME:

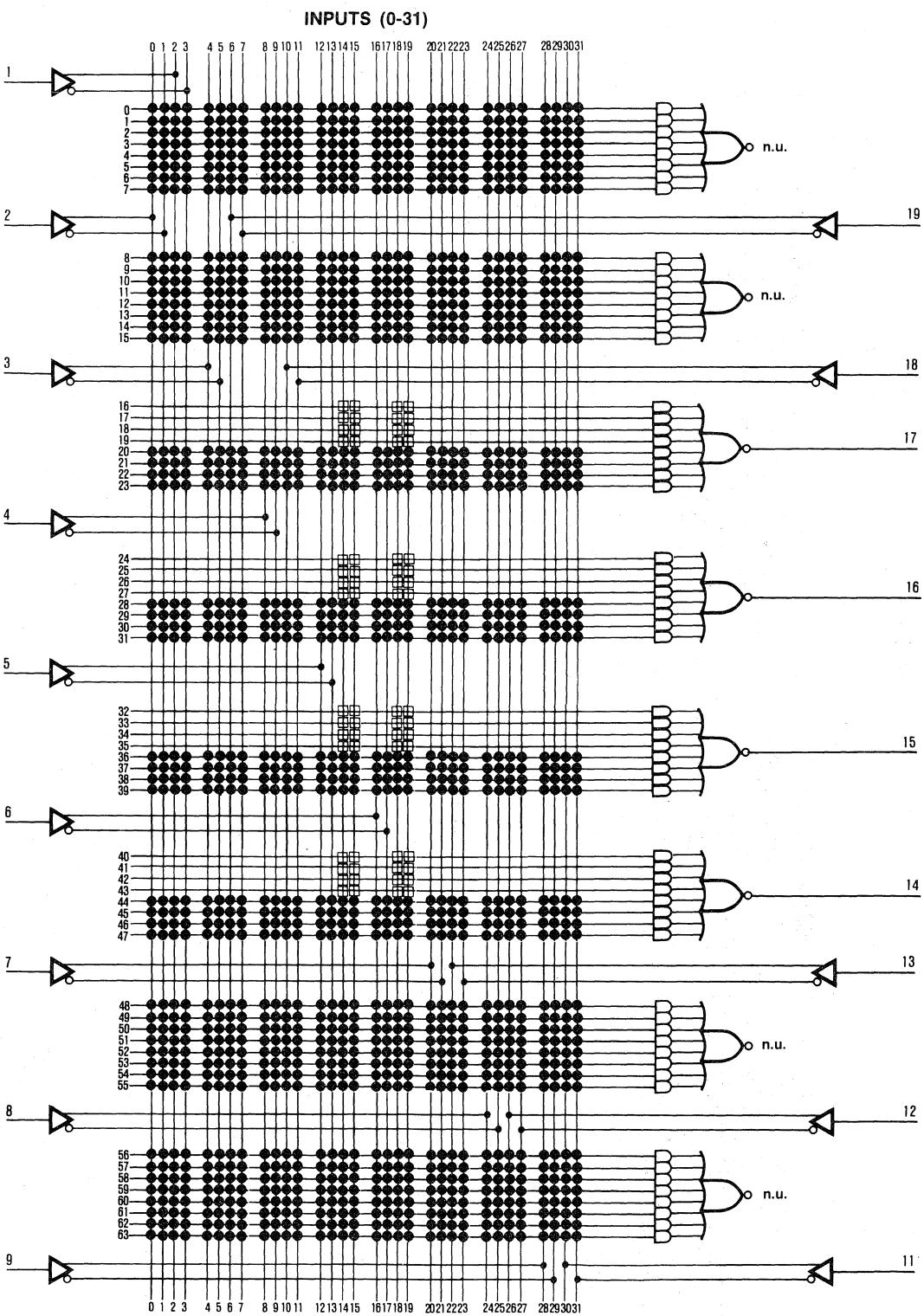
DATE:

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24											H	H			H	H			H	H			H	H								
O_3 16											H	H			H	H			H	H			H	H								
O_2 8											H	H			H	H			H	H			H	H								
O_1 0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25											H	H			H	H			H	H			H	H								
O_3 17											H	H			H	H			H	H			H	H								
O_2 9											H	H			H	H			H	H			H	H								
O_1 1	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 18	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 10											H	H			H	H			H	H			H	H								
O_1 2	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 19	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 11											H	H			H	H			H	H			H	H								
O_1 3	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 13	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 5	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 14	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 6	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 7	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 48											H	H			H	H			H	H			H	H								
O_2 40											H	H			H	H			H	H			H	H								
O_1 32											H	H			H	H			H	H			H	H								
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 49											H	H			H	H			H	H			H	H								
O_2 41											H	H			H	H			H	H			H	H								
O_1 33											H	H			H	H			H	H			H	H								
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 50											H	H			H	H			H	H			H	H								
O_2 42	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 34	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 51											H	H			H	H			H	H			H	H								
O_2 43	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 35	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

6



LEGEND: ● : Phantom Fuse (L, N, 0) □ : Phantom Fuse (H, P, 1) n.u. — not used

PAL14L4

PATTERN: _____

NAME: _____

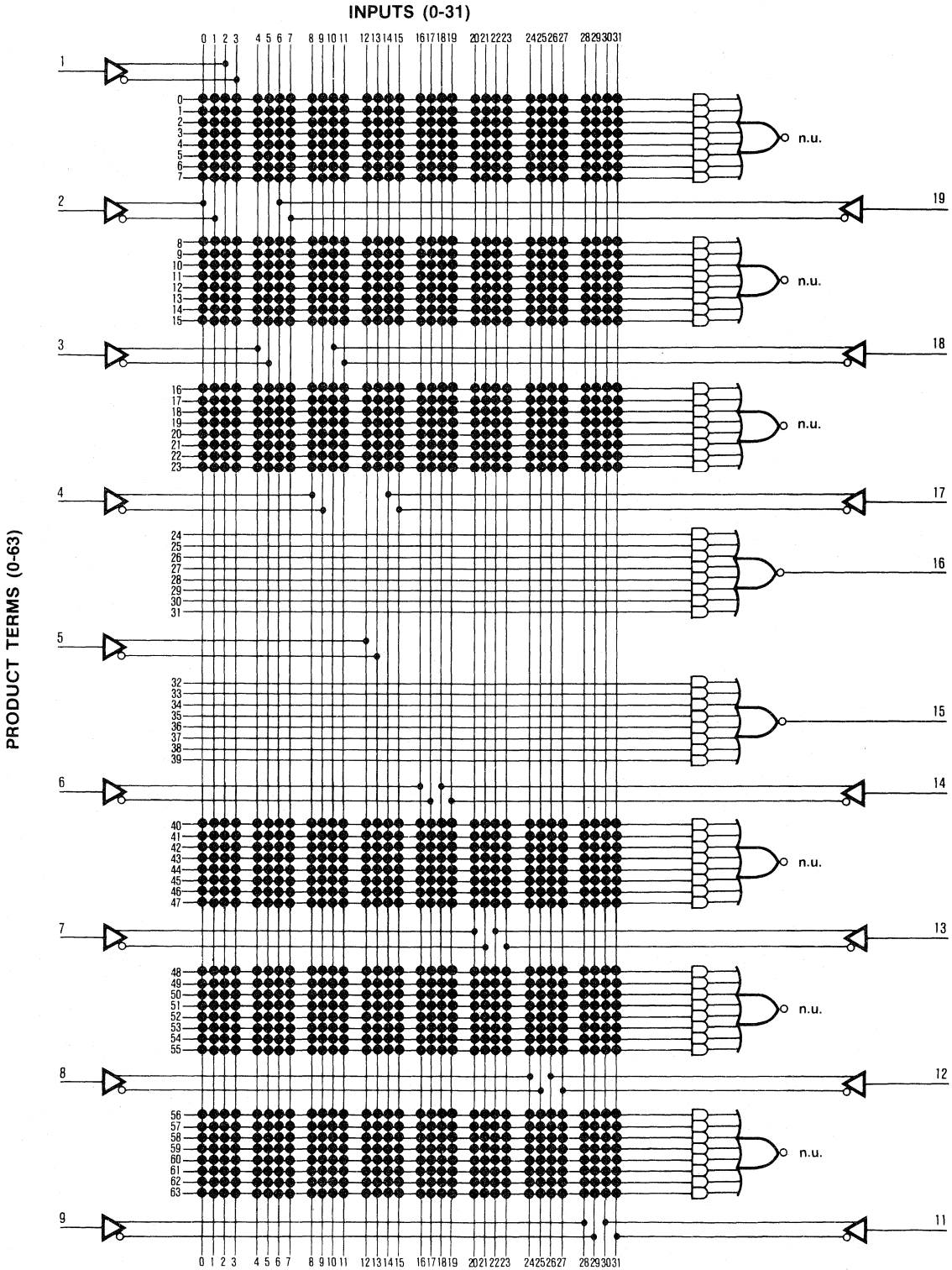
DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24															H	H			H	H												
O_3 16															H	H			H	H												
O_2 8	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25															H	H			H	H												
O_3 17															H	H			H	H												
O_2 9	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 1	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26															H	H			H	H												
O_3 18															H	H			H	H												
O_2 10	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 2	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27															H	H			H	H												
O_3 19															H	H			H	H												
O_2 11	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 3	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 13	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 5	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 14	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 6	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 7	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 48	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 40															H	H			H	H												
O_1 32															H	H			H	H												
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 49	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 41															H	H			H	H												
O_1 33															H	H			H	H												
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 50	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 42															H	H			H	H												
O_1 34															H	H			H	H												
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 51	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 43															H	H			H	H												
O_1 35															H	H			H	H												
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

6



LEGEND: ● : Phantom Fuse (L, N, 0) □ : Phantom Fuse (H, P, 1) n.u. — not used

Programming Format

PAL16L2

PATTERN: _____

NAME: _____

DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24																																
O_3 16	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 8	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25																																
O_3 17	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 9	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 1	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26																																
O_3 18	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 10	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 2	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27																																
O_3 19	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 11	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 3	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28																																
O_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29																																
O_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 13	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 5	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30																																
O_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 14	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 6	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31																																
O_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 7	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 48	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 40	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 49	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 41	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 50	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 42	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 51	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 43	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

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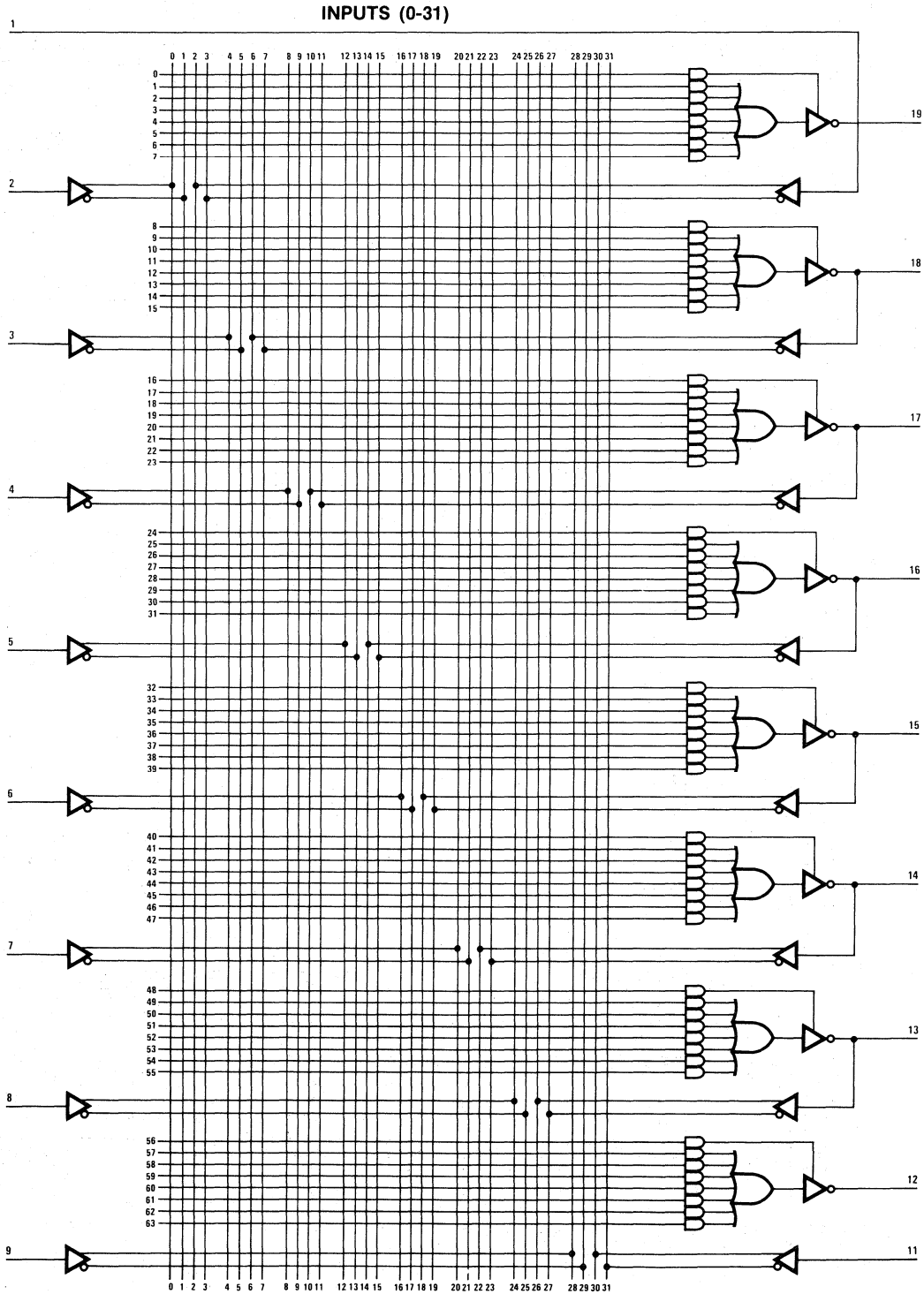
Logic Diagram PAL16L8



PAL16L8

NAME:

PATTERN:

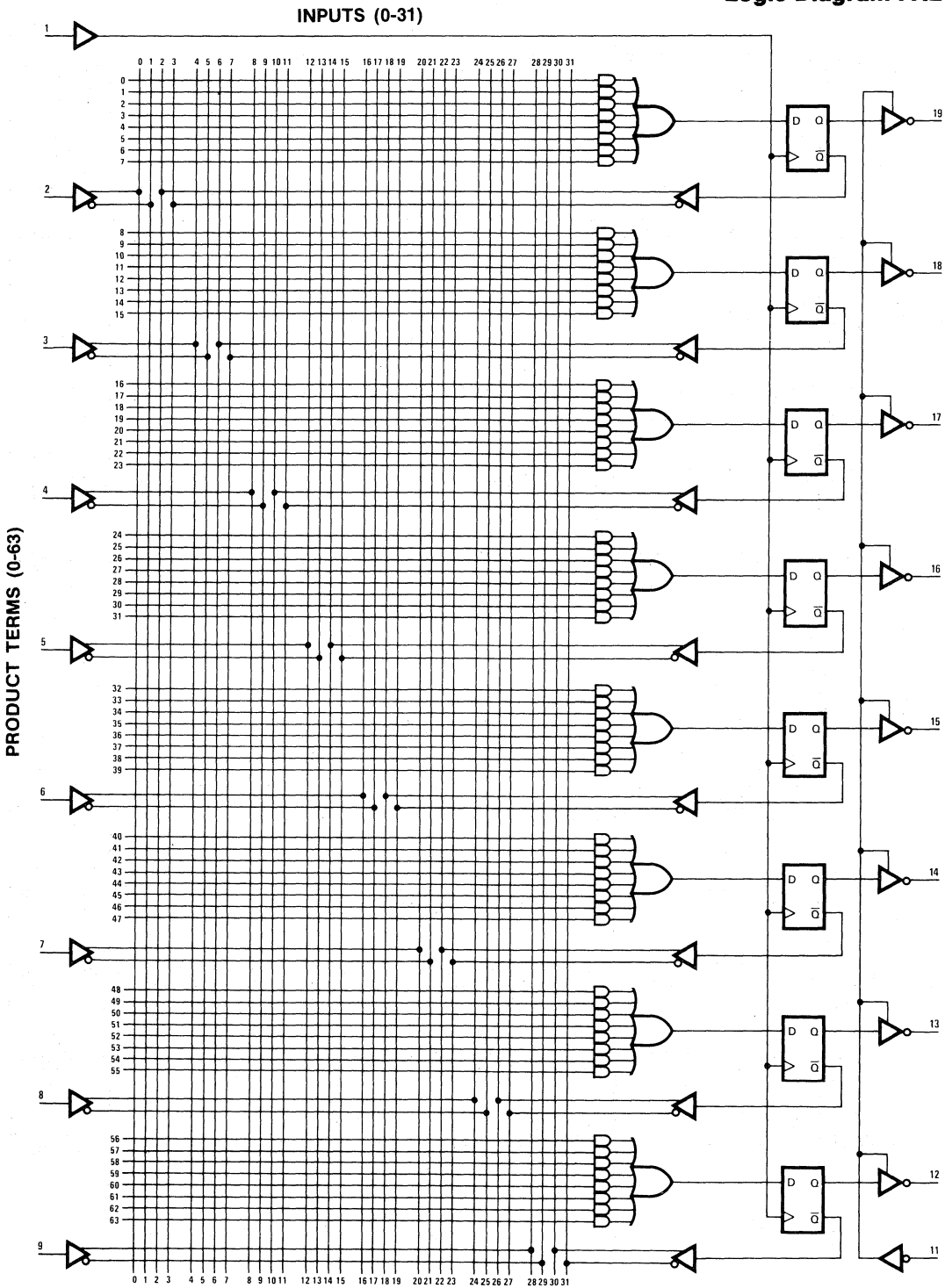
DATE:

INPUTS (0-31)

PRODUCT TERMS (0-63)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24																																
O_3 16																																
O_2 8																																
O_1 0																																
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25																																
O_3 17																																
O_2 9																																
O_1 1																																
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26																																
O_3 18																																
O_2 10																																
O_1 2																																
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27																																
O_3 19																																
O_2 11																																
O_1 3																																
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28																																
O_3 20																																
O_2 12																																
O_1 4																																
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29																																
O_3 21																																
O_2 13																																
O_1 5																																
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30																																
O_3 22																																
O_2 14																																
O_1 6																																
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31																																
O_3 23																																
O_2 15																																
O_1 7																																
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56																																
O_3 48																																
O_2 40																																
O_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57																																
O_3 49																																
O_2 41																																
O_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58																																
O_3 50																																
O_2 42																																
O_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59																																
O_3 51																																
O_2 43																																
O_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60																																
O_3 52																																
O_2 44																																
O_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61																																
O_3 53																																
O_2 45																																
O_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62																																
O_3 54																																
O_2 46																																
O_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63																																
O_3 55																																
O_2 47																																
O_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Logic Diagram PAL16R8



PAL16R8

NAME:

PATTERN:

DATE:

INPUTS (0-31)

PRODUCT TERMS (0-63)

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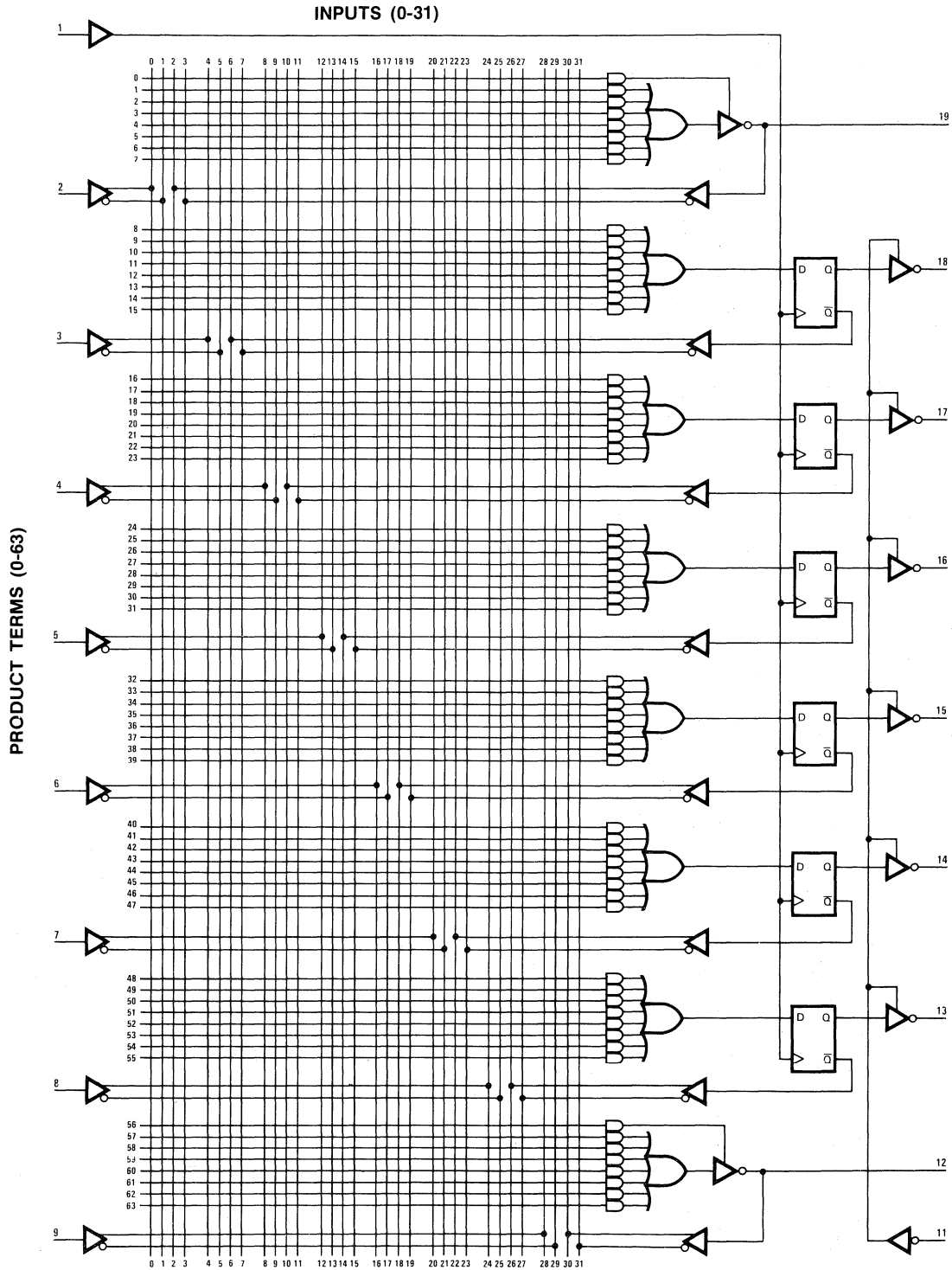
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24																																
O_3 16																																
O_2 8																																
O_1 0																																
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25																																
O_3 17																																
O_2 9																																
O_1 1																																
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26																																
O_3 18																																
O_2 10																																
O_1 2																																
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27																																
O_3 19																																
O_2 11																																
O_1 3																																
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28																																
O_3 20																																
O_2 12																																
O_1 4																																
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29																																
O_3 21																																
O_2 13																																
O_1 5																																
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30																																
O_3 22																																
O_2 14																																
O_1 6																																
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31																																
O_3 23																																
O_2 15																																
O_1 7																																
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56																																
O_3 48																																
O_2 40																																
O_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57																																
O_3 49																																
O_2 41																																
O_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58																																
O_3 50																																
O_2 42																																
O_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59																																
O_3 51																																
O_2 43																																
O_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60																																
O_3 52																																
O_2 44																																
O_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61																																
O_3 53																																
O_2 45																																
O_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62																																
O_3 54																																
O_2 46																																
O_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63																																
O_3 55																																
O_2 47																																
O_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Logic Diagram PAL16R6



PAL16R6

NAME:

PATTERN:

DATE:

PRODUCT TERMS (0-63)

INPUTS (0-31)

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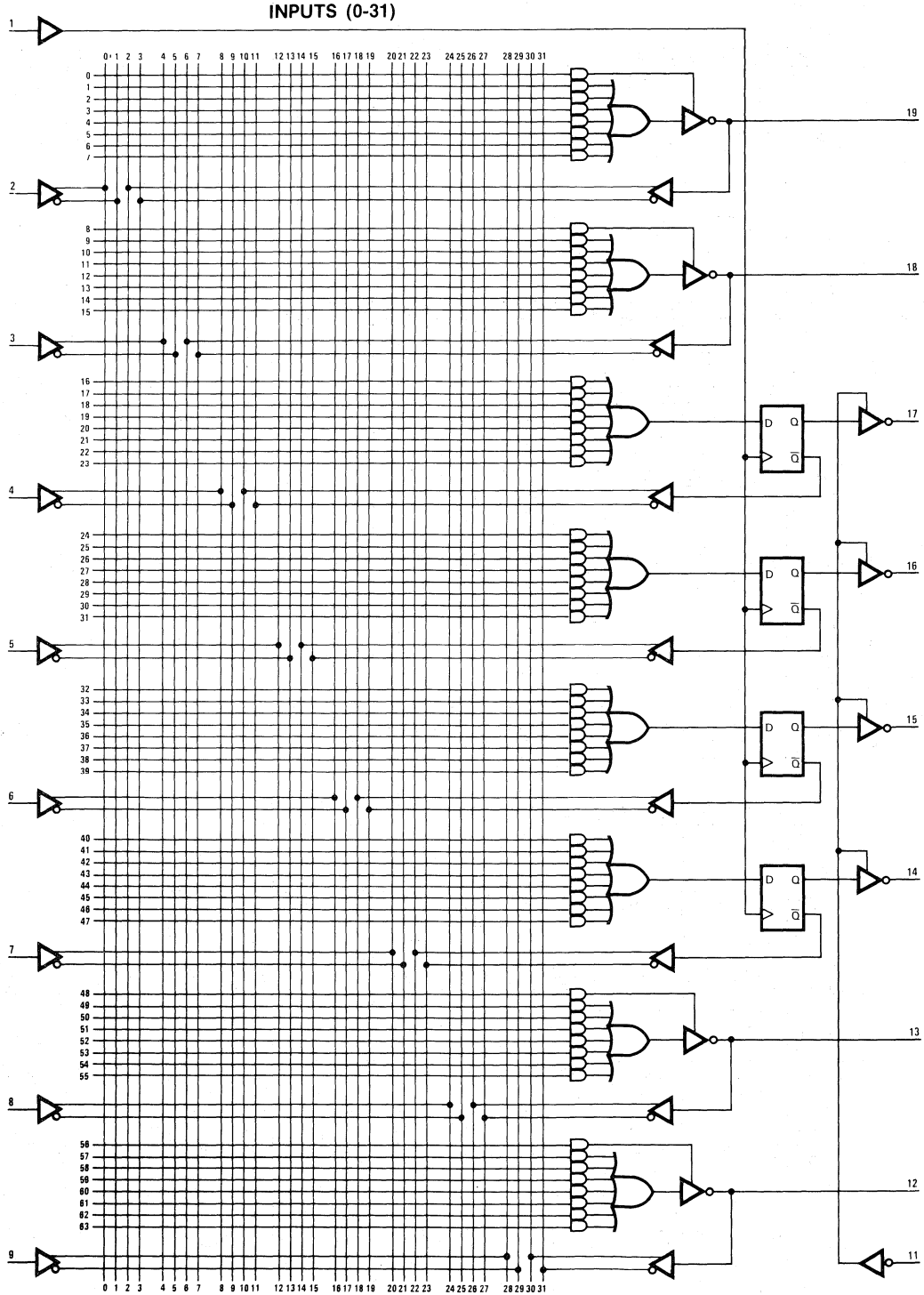
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24																																
O_3 16																																
O_2 8																																
O_1 0																																
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25																																
O_3 17																																
O_2 9																																
O_1 1																																
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26																																
O_3 18																																
O_2 10																																
O_1 2																																
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27																																
O_3 19																																
O_2 11																																
O_1 3																																
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28																																
O_3 20																																
O_2 12																																
O_1 4																																
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29																																
O_3 21																																
O_2 13																																
O_1 5																																
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30																																
O_3 22																																
O_2 14																																
O_1 6																																
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31																																
O_3 23																																
O_2 15																																
O_1 7																																
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56																																
O_3 48																																
O_2 40																																
O_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57																																
O_3 49																																
O_2 41																																
O_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58																																
O_3 50																																
O_2 42																																
O_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59																																
O_3 51																																
O_2 43																																
O_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60																																
O_3 52																																
O_2 44																																
O_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61																																
O_3 53																																
O_2 45																																
O_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62																																
O_3 54																																
O_2 46																																
O_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63																																
O_3 55																																
O_2 47																																
O_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Logic Diagram PAL16R4



PAL16R4

NAME:

PATTERN:

DATE:

PRODUCT TERMS (0-63)

INPUTS (0-31)

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WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24																																
O_3 16																																
O_2 8																																
O_1 0																																
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25																																
O_3 17																																
O_2 9																																
O_1 1																																
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26																																
O_3 18																																
O_2 10																																
O_1 2																																
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27																																
O_3 19																																
O_2 11																																
O_1 3																																
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28																																
O_3 20																																
O_2 12																																
O_1 4																																
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29																																
O_3 21																																
O_2 13																																
O_1 5																																
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30																																
O_3 22																																
O_2 14																																
O_1 6																																
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31																																
O_3 23																																
O_2 15																																
O_1 7																																
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56																																
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O_2 40																																
O_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57																																
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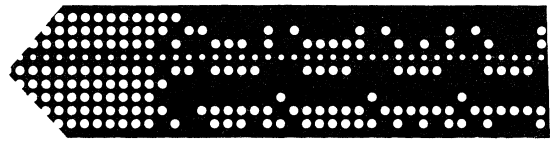
O_2 41																																
O_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58																																
O_3 50																																
O_2 42																																
O_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59																																
O_3 51																																
O_2 43																																
O_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60																																
O_3 52																																
O_2 44																																
O_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61																																
O_3 53																																
O_2 45																																
O_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62																																
O_3 54																																
O_2 46																																
O_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63																																
O_3 55																																
O_2 47																																
O_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

6

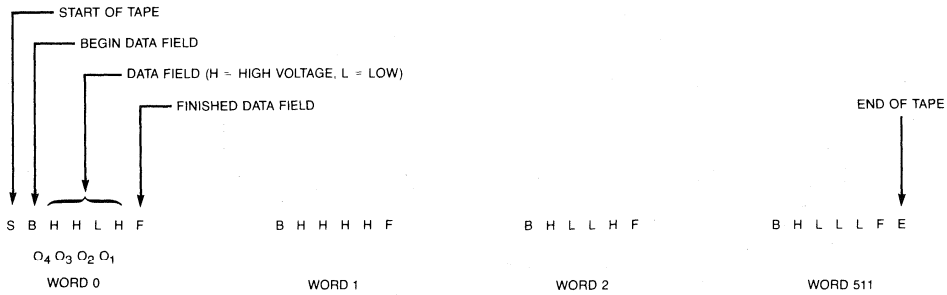
Paper Tape Inputs

Truth tables can be sent to MMI in an ASCII tape format. Information can be sent by mail or TWX. (MMI's TWX number is 910-339-9229.) Although MMI can program PALs with the tape in any format, the following formats have been the most popular.

8 Level TWX



BHLF Format



The required heading information at the beginning of the tape is as follows:

CUSTOMER'S NAME AND PHONE _____
CUSTOMER'S TWX NUMBER (IF ANY) _____
PURCHASE ORDER NUMBER _____
MMI PART NUMBER _____
CUSTOMER SYMBOLIZED PART NUMBER _____
TRUTH TABLE NUMBER (IF ANY) _____
TYPE OF FORMAT (IF ASCII, HEX, BHLF, ETC.) _____
25 BELL OR RUBOUT CHARACTERS _____

An example is shown below:

```
BLARNEY ELECTRONICS  408-735-8104
TWX911-338-9225
PO142
PAL16R8
0431
PAT0001
BHLF
```

(25 Bell or Rubout Characters)

```
S
BLLLHF BLLLLF BLHLHF BLHHHF BLLHHF BHHHHF BLLLHF BLHLHF
   .      .      .      .      .      .      .      .
   .      .      .      .      .      .      .      .
   .      .      .      .      .      .      .      .
   .      .      .      .      .      .      .      .
   .      .      .      .      .      .      .      .
BLLLLF BLHLHF BLHHHF BLLHHF BHHHHF BLLLHF BLHLHF BLLLLF
E
```

BPNF Format

This format is identical to the BHLF format with the exception that a "P" designates a positive bit, and hence a "high" level, and an "N" represents a negative bit, and hence a "low" level.

Hexadecimal Format

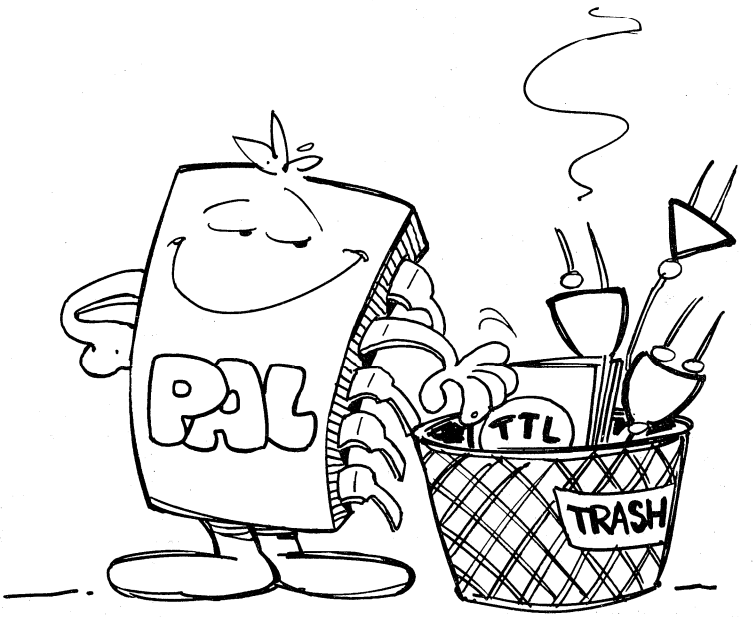
In this format the heading required is identical to the BHLF format but the data is different. Instead of an "S," the hexadecimal data begins with the SOH or STX character (control A). The data is then represented by the hexadecimal character (0-9 and A-F) which represents the output data of address 0, followed by a space.

Next comes the output data of address 1 followed by a space, etc. The character ETX (control C) is used to end the data. Carriage return and line feed may be included to format the data when the tape is printed.

Decimal to Hexadecimal Conversion Table

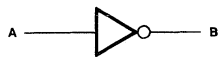
DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX
0	0	32	20	64	40	96	60	128	80	160	A0	192	C0	244	E0	256	100	288	120	320	140	352	160	384	180	416	1A0	448	1C0	480	1E0
1	1	33	21	65	41	97	61	129	81	161	A1	193	C1	225	E1	257	101	289	121	321	141	353	161	385	181	417	1A1	449	1C1	481	1E1
2	2	34	22	66	42	98	62	130	82	162	A2	194	C2	226	E2	258	102	290	122	322	142	354	162	386	182	418	1A2	450	1C2	482	1E2
3	3	35	23	67	43	99	63	131	83	163	A3	195	C3	227	E3	259	103	291	123	323	143	355	163	387	183	419	1A3	451	1C3	483	1E3
4	4	36	24	68	44	100	64	132	84	164	A4	196	C4	228	E4	260	104	292	124	324	144	356	164	388	184	420	1A4	452	1C4	484	1E4
5	5	37	25	69	45	101	65	133	85	165	A5	197	C5	229	E5	261	105	293	125	325	145	357	165	389	185	421	1A5	453	1C5	485	1E5
6	6	38	26	70	46	102	66	134	86	166	A6	198	C6	230	E6	262	106	294	126	326	146	358	166	390	186	422	1A6	454	1C6	486	1E6
7	7	39	27	71	47	103	67	135	87	167	A7	199	C7	231	E7	263	107	295	127	327	147	359	167	391	187	423	1A7	455	1C7	487	1E7
8	8	40	28	72	48	104	68	136	88	168	A8	200	C8	232	E8	264	108	296	128	328	148	360	168	392	188	424	1A8	456	1C8	488	1E8
9	9	41	29	73	49	105	69	137	89	169	A9	201	C9	233	E9	265	109	297	129	329	149	361	169	393	189	425	1A9	457	1C9	489	1E9
10	A	42	2A	74	4A	106	GA	138	8A	170	AA	202	CA	234	EA	266	10A	298	12A	330	14A	362	16A	394	18A	426	1AA	458	1CA	490	IEA
11	B	43	2B	75	4B	107	GB	139	8B	171	AB	203	CB	235	EB	267	10B	299	12B	331	14B	363	16B	395	18B	427	1AB	459	1CB	491	1EB
12	C	44	2C	76	4C	108	GC	140	8C	172	AC	204	CC	236	EC	268	10C	300	12C	332	14C	364	16C	396	18C	428	1AC	460	1CC	492	1EC
13	D	45	2D	77	4D	109	GD	141	8D	173	AD	205	CD	237	ED	269	10D	301	12D	333	14D	365	16D	397	18D	429	1AD	461	1CD	493	1ED
14	E	46	2E	78	4E	110	GE	142	8E	174	AE	206	CE	238	EE	270	10E	302	12E	334	14E	366	16E	398	18E	430	1AE	462	1CE	494	1EE
15	F	47	2F	79	4F	111	GF	143	8F	175	AF	207	CF	239	EF	271	10F	303	12F	335	14F	367	16F	399	18F	431	1AF	463	1CF	495	1EF
16	10	48	30	80	50	112	70	144	90	176	B0	208	D0	240	F0	272	110	304	130	336	150	368	170	400	190	432	1B0	464	1D0	496	1F0
17	11	49	31	81	51	113	71	145	91	177	B1	209	D1	241	F1	273	111	305	131	337	151	369	171	401	191	433	1B1	465	1D1	497	1F1
18	12	50	32	82	52	114	72	146	92	178	B2	210	D2	242	F2	274	112	306	132	338	152	370	172	402	192	434	1B2	466	1D2	498	1F2
19	13	51	33	83	53	115	73	147	93	179	B3	211	D3	243	F3	275	113	307	133	339	153	371	173	403	193	435	1B3	467	1D3	499	1F3
20	14	52	34	84	54	116	74	148	94	180	B4	212	D4	244	F4	276	114	308	134	340	154	372	174	404	194	436	1B4	468	1D4	500	1F4
21	15	53	35	85	55	117	75	149	95	181	B5	213	D5	245	F5	277	115	309	135	341	155	373	175	405	195	437	1B5	469	1D5	501	1F5
22	16	54	36	86	56	118	76	150	96	182	B6	214	D6	246	F6	278	116	310	136	342	156	374	176	406	196	438	1B6	470	1D6	502	1F6
23	17	55	37	87	57	119	77	151	97	183	B7	215	D7	247	F7	279	117	311	137	343	157	375	177	407	197	439	1B7	471	1D7	503	1F7
24	18	56	38	88	58	120	78	152	98	184	B8	216	D8	248	F8	280	118	312	138	344	158	376	178	408	198	440	1B8	472	1D8	504	1F8
25	19	57	39	89	59	121	79	153	99	185	B9	217	D9	249	F9	281	119	313	139	345	159	377	179	409	199	441	1B9	473	1D9	505	1F9
26	1A	58	3A	90	5A	122	7A	154	9A	186	BA	218	DA	250	FA	282	11A	314	13A	346	15A	378	17A	410	19A	442	1BA	474	1DA	506	1FA
27	1B	59	3B	91	5B	123	7B	155	9B	187	BB	219	DB	251	FB	283	11B	315	13B	347	15B	379	17B	411	19B	443	1BB	475	1DB	507	1FB
28	1C	60	3C	92	5C	124	7C	156	9C	188	BC	220	DC	252	FC	284	11C	316	13C	348	15C	380	17C	412	19C	444	1BC	476	1DC	508	1FC
29	1D	61	3D	93	5D	125	7D	157	9D	189	BD	221	DD	253	FD	285	11D	317	13D	349	15D	381	17D	413	19D	445	1BD	477	1DD	509	IFD
30	1E	62	3E	94	5E	126	7E	158	9E	190	BE	222	DE	254	FE	286	11E	318	13E	350	15E	382	17E	414	19E	446	1BE	478	1DE	510	1FE
31	1F	63	3F	95	5F	127	7F	159	9F	191	BF	223	DF	255	FF	287	11F	319	13F	351	15F	383	17F	415	19F	447	1BF	479	1DF	511	1FF

Applications

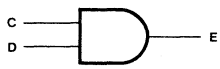


Example 1: Basic Gates

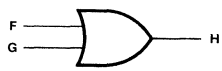
B = /A

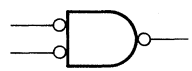


E = C * D

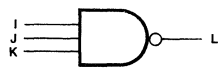


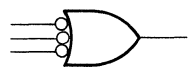
H = F + G





L = /I + /J + /K

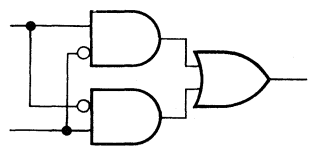




O = /M * /N

R = P:+:Q

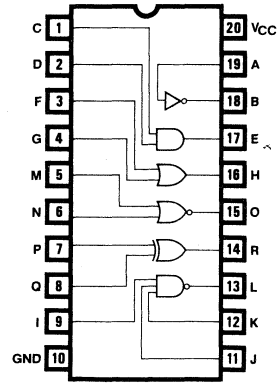
= P * /Q + /P * Q



This example demonstrates how fusable logic can implement the basic inverter, AND, OR, NAND, NOR, and exclusive-OR functions. Note the one to one correspondence between conventional logic symbology and PAL logic symbology. The PAL12H6 is selected because it has 12 inputs and 6 outputs. For this example, the fuse pattern is generated using

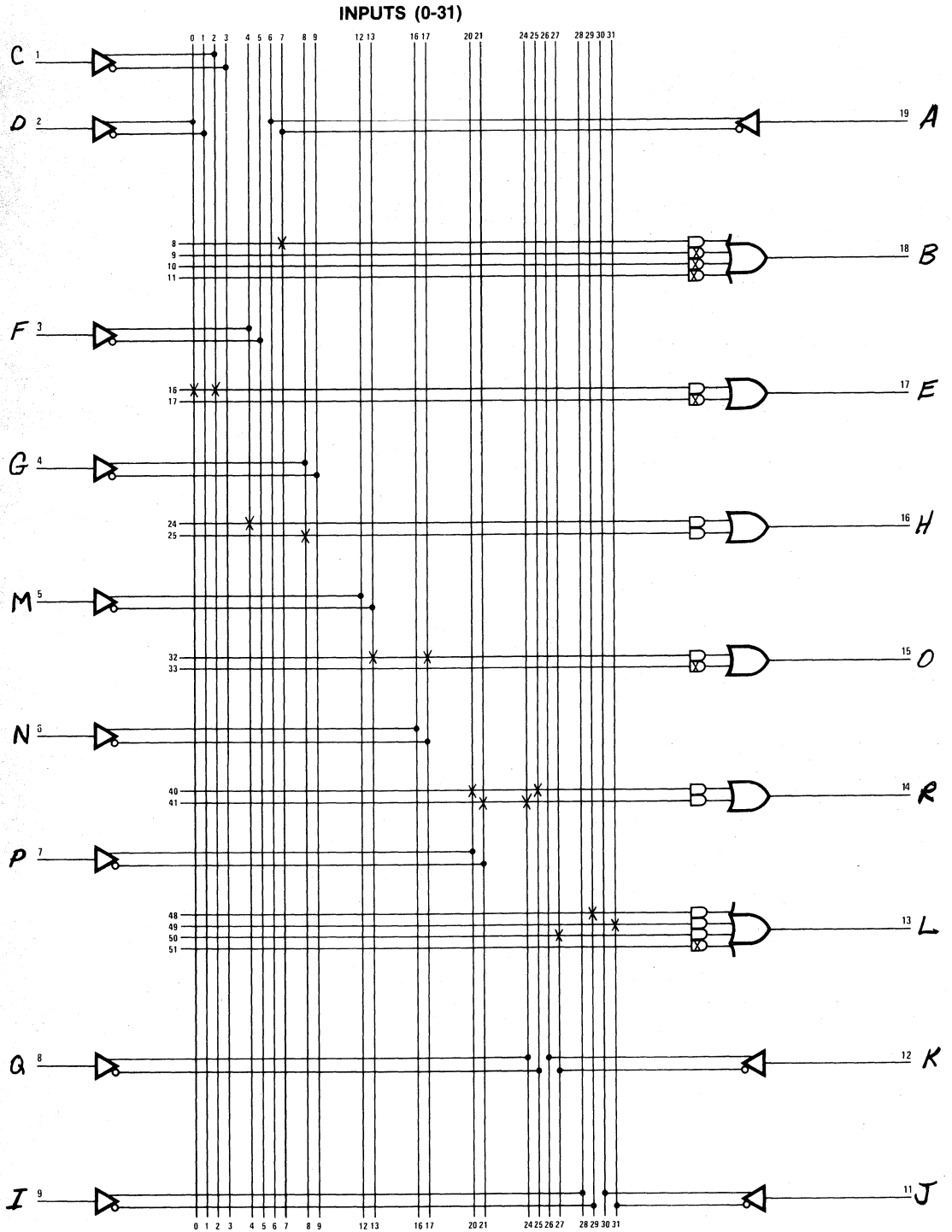
a) PALASM
b) Manual Programming Format (BHLF) Manual Coding

PAL12H6



Basic Gates

Logic Diagram PAL12H6



PALASM Output: Basic Gates

Design Specification PAL12H6

```
*************************** P00211 ****************************
YOUR PAL DESIGN SPEC IS ACCEPTED AS MONOLITHIC MEMORIES BIT
PATTERN NUMBER P00211 . YOUR PASSWORD IS P0055A .
PLEASE CONFIRM THAT THESE EQUATIONS ARE CORRECT. MONOLITHIC
MEMORIES WILL NOT PROCESS A PRODUCTION ORDER WITHOUT PROPER
APPROVAL. USE BP NO. P00211 WHEN PLACING A PROGRAMMING ORDER.
***************************************************************

                    CUSTOMER CONFIRMATION

I HAVE REVIEWED THIS PAL DESIGN SPECIFICATION AND UNDERSTAND
THAT PALS ORDERED BY BIT PATTERN NUMBER P00211 WILL BE
PROGRAMMED AS SPECIFIED BELOW.

CUSTOMER COMPANY NAME _____ CITY,STATE _____

 AUTHORISED SIGNATURE _____      DATE _____

         NAME (PRINT) _____      TITLE _____

RETURN TO MMI 1165 E. ARQUES SUNNYVALE, CA 94086 ATTN:_____
***************************************************************

PAL12H6                              PAL DESIGN SPECIFICATION
P0055A                               KAZMI 11/21/79
BASIC GATES EXAMPLE
S.V. CA
C D F G M N  P Q I GND J K L R O H E B A VCC

 B=/A
 E=C*D
 H=F+G
 O=/M*/N
 R=P*/Q+/P*Q
 L=/I+/J+/K

DESCRIPTION: THIS EXAMPLE ILLUSTRATES THE USE OF FUSIBLE LOGIC TO
             IMPLEMENT THE BASIC GATES.

NUMBER OF FUSES BLOWN =  306
```

PALASM Output

HEX FORMAT

```
B F B F 7 F F D F F F F F F F F F F F F F F F F F F F F F F F .
9 9 9 9 9 9 9 9 1 9 F F 9 9 F F 9 9 F F 9 9 F F 9 9 9 9 9 9 9 9 .
1 1 1 1 1 1 1 1 1 1 3 3 1 1 3 3 1 1 3 3 1 1 3 3 1 1 1 1 1 1 1 1 .
1 1 1 1 1 1 1 1 1 1 3 3 1 1 3 3 1 1 3 3 1 1 3 3 1 1 1 1 1 1 1 1 .
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 .
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 .
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 .
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 .
F F F F F F F F F F F F F E F F F E F F D F F F F D F F F B F F .
E E E E E E E E E E F F E E F F E E F F E C F F C E E E E E E A .
C C C C C C C C C C C C C C C C C C C C C C C C C C 8 C C C C .
8 8 8 8 8 8 8 8 8 8 C C 8 8 C C 8 8 C C 8 8 C C 8 8 8 8 8 8 8 8 .
8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 .
8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 .
8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 .
8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 .
```

PALASM Output: Basic Gates

Fuse Plot PAL12H6

```
                    11 1111 1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0 0000 0000 0000 0000 0000 0000 0000 0000
 1 0000 0000 0000 0000 0000 0000 0000 0000
 2 0000 0000 0000 0000 0000 0000 0000 0000
 3 0000 0000 0000 0000 0000 0000 0000 0000
 4 0000 0000 0000 0000 0000 0000 0000 0000
 5 0000 0000 0000 0000 0000 0000 0000 0000
 6 0000 0000 0000 0000 0000 0000 0000 0000
 7 0000 0000 0000 0000 0000 0000 0000 0000

 8 ---- ---X --00 --00 --00 --00 ---- ---- /A
 9 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
10 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
11 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
12 0000 0000 0000 0000 0000 0000 0000 0000
13 0000 0000 0000 0000 0000 0000 0000 0000
14 0000 0000 0000 0000 0000 0000 0000 0000
15 0000 0000 0000 0000 0000 0000 0000 0000

16 X-X- ---- --00 --00 --00 --00 ---- ---- C*D
17 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
18 0000 0000 0000 0000 0000 0000 0000 0000
19 0000 0000 0000 0000 0000 0000 0000 0000
20 0000 0000 0000 0000 0000 0000 0000 0000
21 0000 0000 0000 0000 0000 0000 0000 0000
22 0000 0000 0000 0000 0000 0000 0000 0000
23 0000 0000 0000 0000 0000 0000 0000 0000

24 ---- X--- --00 --00 --00 --00 ---- ---- F
25 ---- ---- X-00 --00 --00 --00 ---- ---- G
26 0000 0000 0000 0000 0000 0000 0000 0000
27 0000 0000 0000 0000 0000 0000 0000 0000
28 0000 0000 0000 0000 0000 0000 0000 0000
29 0000 0000 0000 0000 0000 0000 0000 0000
30 0000 0000 0000 0000 0000 0000 0000 0000
31 0000 0000 0000 0000 0000 0000 0000 0000

32 ---- ---- --00 -XOO -XOO --00 ---- ---- /M*/N
33 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
34 0000 0000 0000 0000 0000 0000 0000 0000
35 0000 0000 0000 0000 0000 0000 0000 0000
36 0000 0000 0000 0000 0000 0000 0000 0000
37 0000 0000 0000 0000 0000 0000 0000 0000
38 0000 0000 0000 0000 0000 0000 0000 0000
39 0000 0000 0000 0000 0000 0000 0000 0000

40 ---- ---- --00 --00 --00 X-00 -X-- ---- P*/Q
41 ---- ---- --00 --00 --00 -XOO X--- ---- /P*Q
42 0000 0000 0000 0000 0000 0000 0000 0000
43 0000 0000 0000 0000 0000 0000 0000 0000
44 0000 0000 0000 0000 0000 0000 0000 0000
45 0000 0000 0000 0000 0000 0000 0000 0000
46 0000 0000 0000 0000 0000 0000 0000 0000
47 0000 0000 0000 0000 0000 0000 0000 0000

48 ---- ---- --00 --00 --00 --00 ---- -X-- /I
49 ---- ---- --00 --00 --00 --00 ---- ---X /J
50 ---- ---- --00 --00 --00 --00 ---X ---- /K
51 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
52 0000 0000 0000 0000 0000 0000 0000 0000
53 0000 0000 0000 0000 0000 0000 0000 0000
54 0000 0000 0000 0000 0000 0000 0000 0000
55 0000 0000 0000 0000 0000 0000 0000 0000

56 0000 0000 0000 0000 0000 0000 0000 0000
57 0000 0000 0000 0000 0000 0000 0000 0000
58 0000 0000 0000 0000 0000 0000 0000 0000
59 0000 0000 0000 0000 0000 0000 0000 0000
60 0000 0000 0000 0000 0000 0000 0000 0000
61 0000 0000 0000 0000 0000 0000 0000 0000
62 0000 0000 0000 0000 0000 0000 0000 0000
63 0000 0000 0000 0000 0000 0000 0000 0000


LEGEND:  X : FUSE NOT BLOWN (L,N,0)    - : FUSE BLOWN    (H,P,1)
         0 : PHANTOM FUSE   (L,N,0)    O : PHANTOM FUSE (H,P,1)
```

PALASM Output: Basic Gates

BHLF Format PAL12H6

```
BHLHHF BHHHHF BHLHHF BHHHHF BLHHHF BHHHHF BHHHHF BHHLHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF
BLLLHF BHLLHF BHHHHF BHHHHF BHLLHF BHLLHF BHHHHF BHHHHF
BHLLHF BHLLHF BHHHHF BHHHHF BHLLHF BHLLHF BHHHHF BHHHHF
BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLHHF BLLHHF BLLLHF BLLLHF BLLHHF BLLHHF
BLLLHF BLLLHF BLLHHF BLLHHF BLLLHF BLLLHF BLLHHF BLLHHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLHHF BLLHHF BLLLHF BLLLHF BLLHHF BLLHHF
BLLLHF BLLLHF BLLHHF BLLHHF BLLLHF BLLLHF BLLHHF BLLHHF
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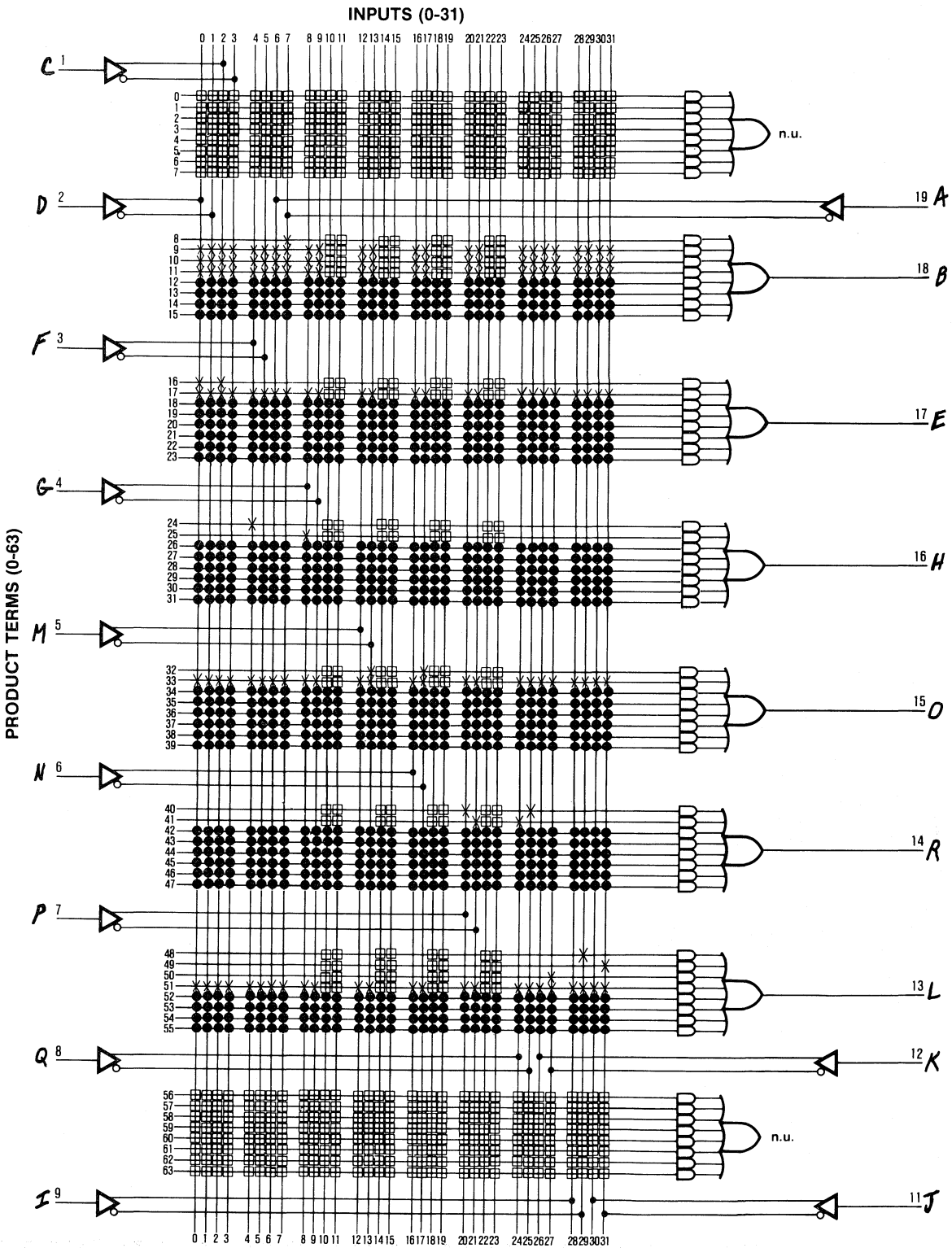


LEGEND: ● : Phantom Fuse (L, N, 0) □ : Phantom Fuse (H, P, 1) n.u. — not used

PAL12H6

PATTERN: POOSSA

NAME: S. KAZMI

DATE: 11-21-79

Programming Format

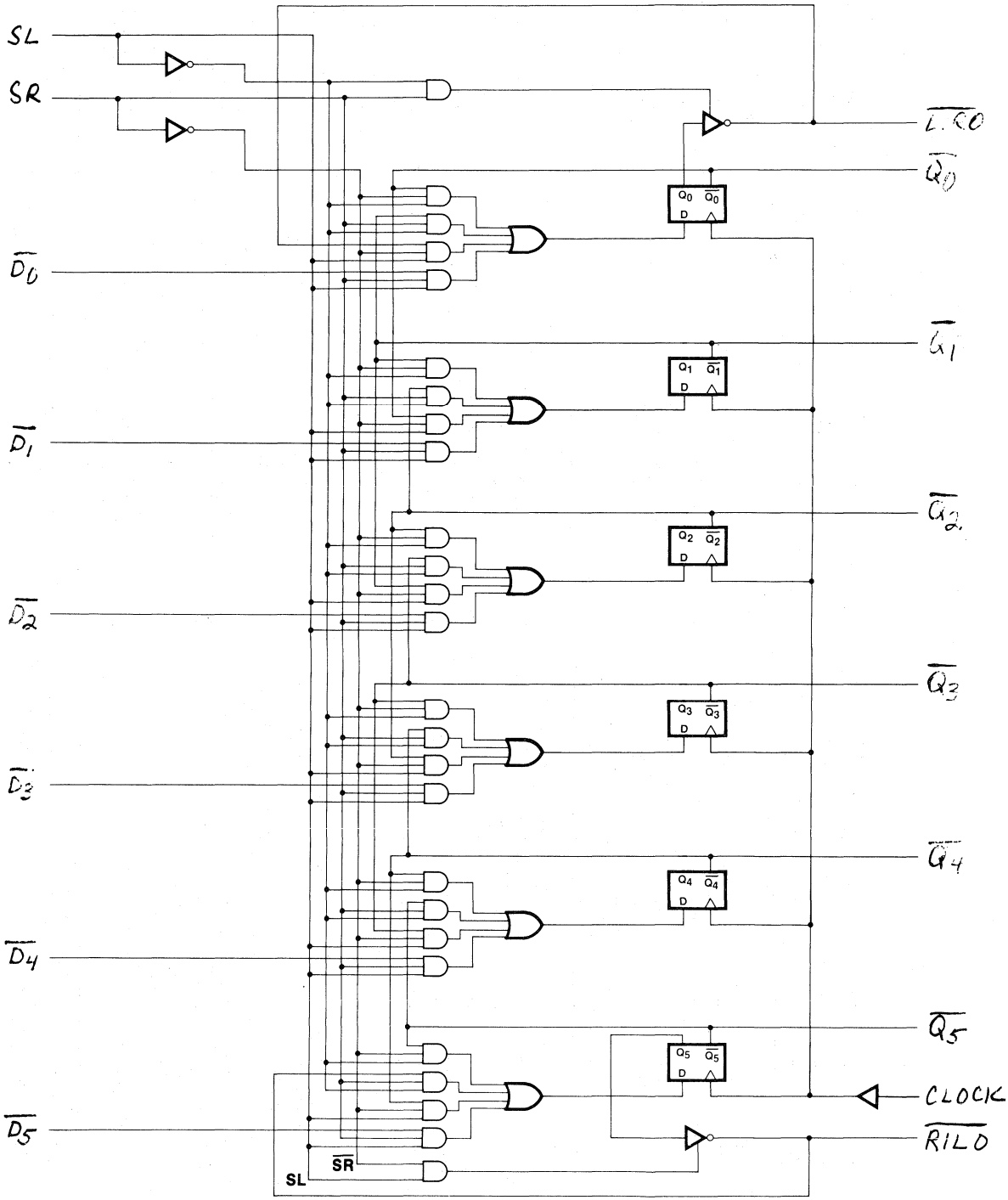
PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 16	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 8	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 17	L	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	L
O_2 9	L	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	L
O_1 1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 18	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 10	L	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	L
O_1 2	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 19	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 11	L	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	L
O_1 3	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 4	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 13	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 5	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 14	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 6	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 7	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 48	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 40	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	L	H	H	H	H	H	H
O_1 32	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 49	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
O_2 41	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	L	H	H	H	H	H	H	H
O_1 33	L	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	L	L
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 50	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
O_2 42	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 34	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 51	L	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	L
O_2 43	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 35	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

Example 2:

6-Bit Shift Register with Three-State Outputs



PALASM Output: 6-Bit Shift Register with Three-State Outputs

Design Specification PAL16R6

```
****************************** P00206 ******************************
YOUR PAL DESIGN SPEC IS ACCEPTED AS MONOLITHIC MEMORIES BIT
PATTERN NUMBER P00206 . YOUR PASSWORD IS PAT0005 .
PLEASE CONFIRM THAT THESE EQUATIONS ARE CORRECT. MONOLITHIC
MEMORIES WILL NOT PROCESS A PRODUCTION ORDER WITHOUT PROPER
APPROVAL. USE BP NO. P00206 WHEN PLACING A PROGRAMMING ORDER.
************************************************************************

                        CUSTOMER CONFIRMATION

I HAVE REVIEWED THIS PAL DESIGN SPECIFICATION AND UNDERSTAND
THAT PALS ORDERED BY BIT PATTERN NUMBER P00206 WILL BE
PROGRAMMED AS SPECIFIED BELOW.

CUSTOMER COMPANY NAME _________________  CITY,STATE _____________

 AUTHORISED SIGNATURE _________________        DATE _____________

         NAME (PRINT) _________________       TITLE _____________

RETURN TO MMI 1165 E. ARQUES SUNNYVALE, CA 94086 ATTN:_____________
************************************************************************

PAL16R6                                        PAL DESIGN SPECIFICATION
PAT0005                                          JOHN BIRKNER 11/20/77
6-BIT SHIFT REGISTER WITH THREE-STATE OUTPUTS
MMI,SV
CK SR D0 D1 D2 D3 D4 D5 SL GND /E RILO Q5 Q4 Q3 Q2 Q1 Q0 LIRO VCC

IF(SR*/SL) /LIRO=/Q0
/Q0 := /SR*/SL*/Q0 + SR*/SL*/Q1 + /SR*SL*/LIRO + SR*SL*/D0
/Q1 := /SR*/SL*/Q1 + SR*/SL*/Q2 + /SR*SL*/Q0 + SR*SL*/D1
/Q2 := /SR*/SL*/Q2 + SR*/SL*/Q3 + /SR*SL*/Q1 + SR*SL*/D2
/Q3 := /SR*/SL*/Q3 + SR*/SL*/Q4 + /SR*SL*/Q2 + SR*SL*/D3
/Q4 := /SR*/SL*/Q4 + SR*/SL*/Q5 + /SR*SL*/Q3 + SR*SL*/D4
/Q5 := /SR*/SL*/Q5 + SR*/SL*/RILO + /SR*SL*/Q4 + SR*SL*/D5
IF(/SR*SL) /RILO=/Q5

DESCRIPTION:
THE 6-BIT SHIFT REGISTER WILL HOLD , SHIFT RIGHT, SHIFT LEFT, OR LOAD
ON THE RISING EDGE OF THE CLOCK (CK).
THE THREE STATE OUTPUTS ARE HIGH-Z WHEN THE ENABLE LINE (/E) IS HIGH AND
ENABLED WHEN ENABLE LINE (/E) IS LOW.
FUNCTION TABLE:
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INPUTS						OUTPUTS							
SL	SR	RILO	LIRO	CLOCK	RILO	Q5	Q4	Q3	Q2	Q1	Q0	LIRO	OPERATION
L	L	X	X	L-H	Z	Q5	Q4	Q3	Q2	Q1	Q0	Z	HOLD
L	H	RI	X	L-H	Z	RI	Q5	Q4	Q3	Q2	Q1	Q1	RIGHT SHFT
H	L	X	LI	L-H	Q4	Q4	Q3	Q2	Q1	Q0	LI	Z	LEFT SHFT
H	H	X	X	L-H	Z	D5	D4	D3	D2	D1	D0	Z	LOAD D

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NUMBER OF FUSES BLOWN =  818
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PALASM Output HEX FORMAT

```
E 1 F F F F F D F F F B F F F 7 F F F F F F F F F F F 0 F F .
1 F F F F F F E F F F D F F F B F F F 7 F F F F F F F F F 1 F F .
E 0 E C E E E A E E E 6 E E E E E E E E E E E E E E E 0 E E E .
0 E E E E C E E E A E E E 6 E E E E E E E E E E E E E 0 E E E .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
F 0 F F F F F F F F F F F F F F F F F F F F F F F F F F F F F .
8 F F F F F F F F F F F F F F F F F F F F F F F F F F F F F B .
7 0 7 7 7 7 7 7 7 7 7 7 7 7 7 6 7 7 7 5 7 7 7 3 7 7 7 7 0 7 7 7 .
0 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 6 7 7 7 5 7 7 7 3 7 7 0 7 7 7 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
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0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
```

PALASM Output: 6-Bit Shift Register with Three-State Outputs

Fuse Plot PAL16R6

```
                    11 1111 1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0 X--- ---- ---- ---- ---- ---- ---- -X-- SR*/SL
 1 ---- ---X ---- ---- ---- ---- ---- ---- /Q0
 2 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 3 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 4 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 5 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 6 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 7 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

 8 -X-- ---X ---- ---- ---- ---- ---- -X-- /SR*/SL*/Q0
 9 X--- ---- ---X ---- ---- ---- ---- -X-- SR*/SL*/Q1
10 -X-X ---- ---- ---- ---- ---- ---- X--- /SR*SL*/LIRO
11 X--- -X-- ---- ---- ---- ---- ---- X--- SR*SL*/D0
12 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
13 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
14 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
15 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

16 -X-- ---- ---X ---- ---- ---- ---- -X-- /SR*/SL*/Q1
17 X--- ---- ---- ---X ---- ---- ---- -X-- SR*/SL*/Q2
18 -X-- ---X ---- ---- ---- ---- ---- X--- /SR*SL*/Q0
19 X--- ---- -X-- ---- ---- ---- ---- X--- SR*SL*/D1
20 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
21 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
22 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
23 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

24 -X-- ---- ---- ---X ---- ---- ---- -X-- /SR*/SL*/Q2
25 X--- ---- ---- ---- ---X ---- ---- -X-- SR*/SL*/Q3
26 -X-- ---- ---X ---- ---- ---- ---- X--- /SR*SL*/Q1
27 X--- ---- ---- -X-- ---- ---- ---- X--- SR*SL*/D2
28 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
29 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
30 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
31 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

32 -X-- ---- ---- ---- ---X ---- ---- -X-- /SR*/SL*/Q3
33 X--- ---- ---- ---- ---- ---X ---- -X-- SR*/SL*/Q4
34 -X-- ---- ---- ---X ---- ---- ---- X--- /SR*SL*/Q2
35 X--- ---- ---- ---- -X-- ---- ---- X--- SR*SL*/D3
36 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
37 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
38 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
39 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

40 -X-- ---- ---- ---- ---- ---X ---- -X-- /SR*/SL*/Q4
41 X--- ---- ---- ---- ---- ---- ---X -X-- SR*/SL*/Q5
42 -X-- ---- ---- ---- ---X ---- ---- X--- /SR*SL*/Q3
43 X--- ---- ---- ---- ---- -X-- ---- X--- SR*SL*/D4
44 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
45 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
46 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
47 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

48 -X-- ---- ---- ---- ---- ---- ---X -X-- /SR*/SL*/Q5
49 X--- ---- ---- ---- ---- ---- ---- -X-X SR*/SL*/RILO
50 -X-- ---- ---- ---- ---- ---X ---- X--- /SR*SL*/Q4
51 X--- ---- ---- ---- ---- ---- -X-- X--- SR*SL*/D5
52 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
53 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
54 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
55 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

56 -X-- ---- ---- ---- ---- ---- ---- X--- /SR*SL
57 ---- ---- ---- ---- ---- ---- ---X ---- /Q5
58 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
59 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
60 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
61 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
62 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
63 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

LEGEND:  X : FUSE NOT BLOWN (L,N,0)    - : FUSE BLOWN    (H,P,1)
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PALASM Output: 6-Bit Shift Register with Three-State Outputs

BHLF Format PAL16R6

```
BHHHLF BLLLHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHLHF
BHHHHF BHHHHF BHHHHF BHLHHF BHHHHF BHHHHF BHHHHF BLHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BLLLLF BHHHHF BHHHHF
BLLLHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHLF
BHHHHF BHHHHF BHHHHF BHHLHF BHHHHF BHHHHF BHHHHF BHLHHF
BHHHHF BHHHHF BHHHHF BLHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BLLLHF BHHHHF BHHHHF
BHHHLF BLLLLF BHHHLF BHHLLF BHHHLF BHHHLF BHHHLF BHLHLF
BHHHLF BHHHLF BHHHLF BLHHLF BHHHLF BHHHLF BHHHLF BHHHLF
BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF
BHHHLF BHHHLF BHHHLF BHHHLF BLLLLF BHHHLF BHHHLF BHHHLF
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BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
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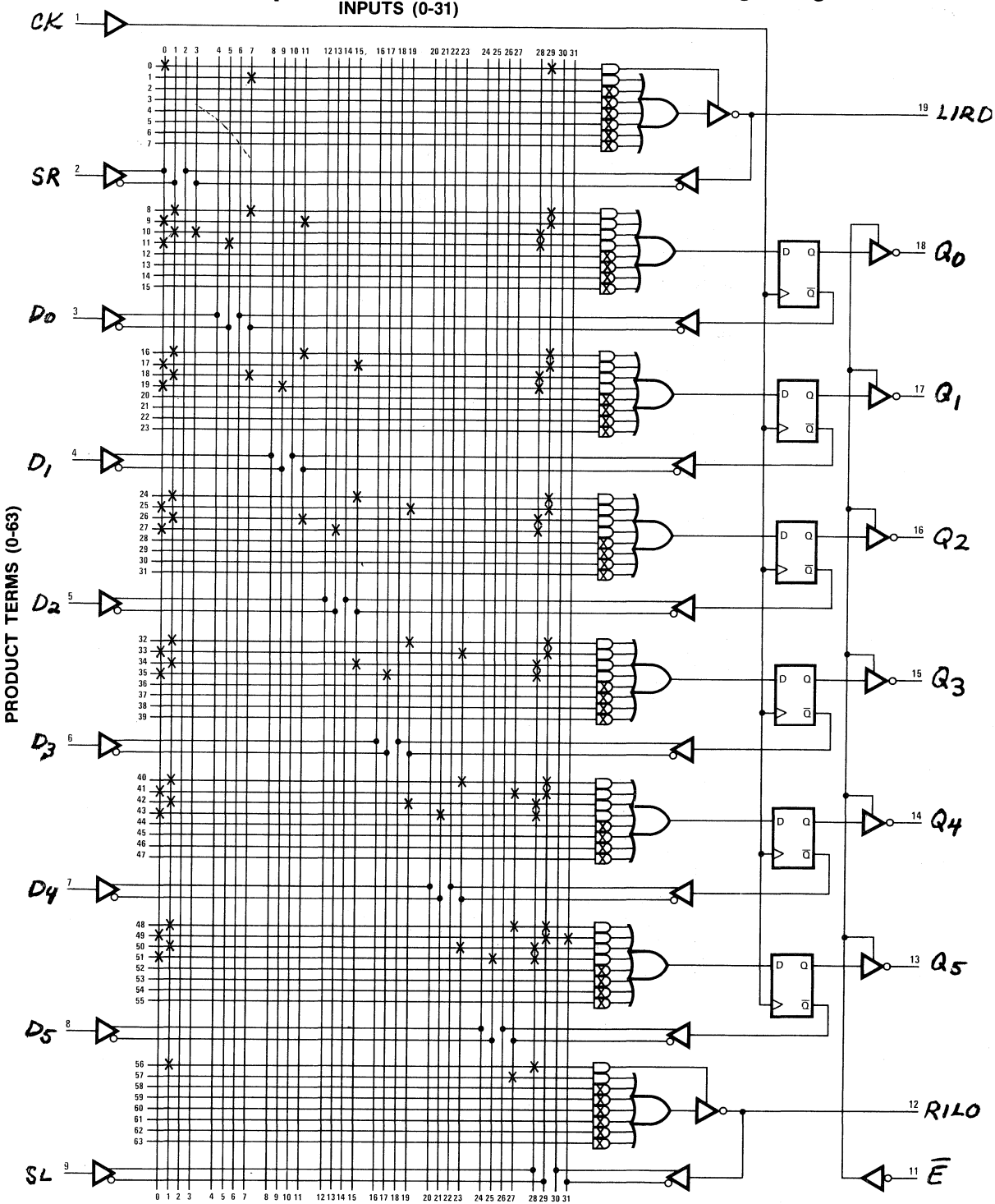
Manual Coding: 6-Bit Shift Register with Three-State Outputs

Logic Diagram PAL16R6



Manual Coding: 6-Bit Shift Register with Three-State Outputs

PAL 16R6 P0005

PATTERN:

NAME: John Birkner

DATE: 11-20-77

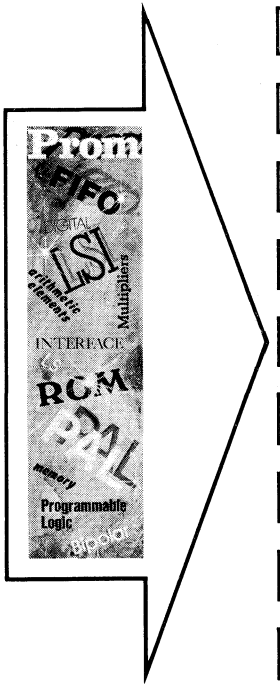
Programming Format

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
O_3 16	H	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
O_2 8	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
O_1 0	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	L	H	H
O_3 17	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	L	H	H
O_2 9	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
O_1 1	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26	H	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
O_3 18	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
O_2 10	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
O_1 2	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
O_3 19	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
O_2 11	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
O_1 3	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 13	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 5	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 14	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 6	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 7	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
O_3 48	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	L	H	H
O_2 40	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	L	H	H
O_1 32	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	L	H	H
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
O_3 49	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	L	H	L
O_2 41	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	L	H	L	H	H
O_1 33	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	L	H	H
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 50	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	L	H	H	H
O_2 42	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H	H	H
O_1 34	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 51	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
O_2 43	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	L	H	H	H
O_1 35	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

6



First-In First-Out (FIFO) 64x4 Serial Memory

57/67401

U.S. Patent 4151609

Features/Benefits

- 10 MHz shift in, shift out guaranteed rates
- TTL inputs and outputs
- Readily expandable in word and bit dimensions
- Output pins directly opposite corresponding input pins
- Asynchronous or synchronous operation
- Pin compatible with Fairchild's F3341 MOS FIFO and ten times as fast

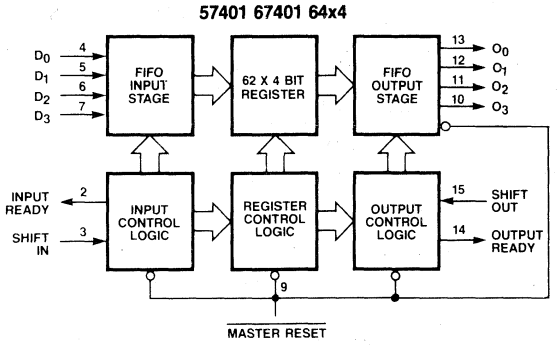
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE RANGE
57401	J16	Military
67401	J16	Commercial

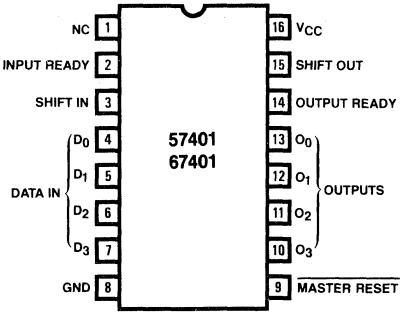
Description

The 67401 is an expandable "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4-bit. A 10 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0-D_3, MR	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		VCC = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current *		V_{CC} = 6V	V_O = 0.5V	−20		−90	mA
I_{CC}	Supply current		V_{CC} = MAX	57401			150	mA
				67401			160	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY		COMMERCIAL		UNIT
			MIN	MAX	MIN	MAX	
f_{IN}	Shift In rate	1	7		10		MHz
t_{SIH}	Shift In HIGH time	1	45		35		ns
t_{SIL}	Shift In LOW time	1	45		35		ns
t_{IRL}	Shift In to input ready LOW	1		60		45	ns
t_{IRH}	Shift In to input ready HIGH	1		60		45	ns
t_{IDS}	Input data set up	1	10		5		ns
t_{IDH}	Input data hold time	1	55		45		ns
f_{OUT}	Shift Out rate	6	7		10		MHz
t_{SOH}	Shift Out HIGH time	6	45		35		ns
t_{SOL}	Shift Out LOW time	6	45		35		ns
t_{ORL}	Shift Out to Output Ready LOW	6		65		55	ns
t_{ORH}	Shift Out to Output Ready HIGH	6		65		55	ns
t_{OD}	Output data delay	6	10	65	10	55	ns
t_{PT}	Data throughput time	4, 9		4		3	μs
t_{MRW}	Master Reset pulse*	11	30		35		ns
t_{MRORL}	Master Reset to OR LOW	11		65		60	ns
t_{MRIRH}	Master Reset to IR HIGH	11		65		60	ns
t_{MRS}	Master Reset to SI	11	45		35		ns
t_{IPH}	Input Ready pulse HIGH	4	20		20		ns
t_{OPH}	Output Ready pulse HIGH	9	20		20		ns

*Master reset clears all the cells to the empty state, and the data-outputs to a LOW-state.

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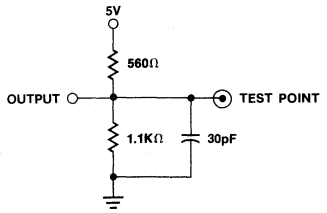
Standard Test Load



Functional Description

Data Input

Data is entered into the FIFO on D0-D3 inputs. To enter data the Input Ready (IR) should be HIGH, indicating that the first location is ready to accept data. Data then present at the four data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O0-O3 outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_{0-3} remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

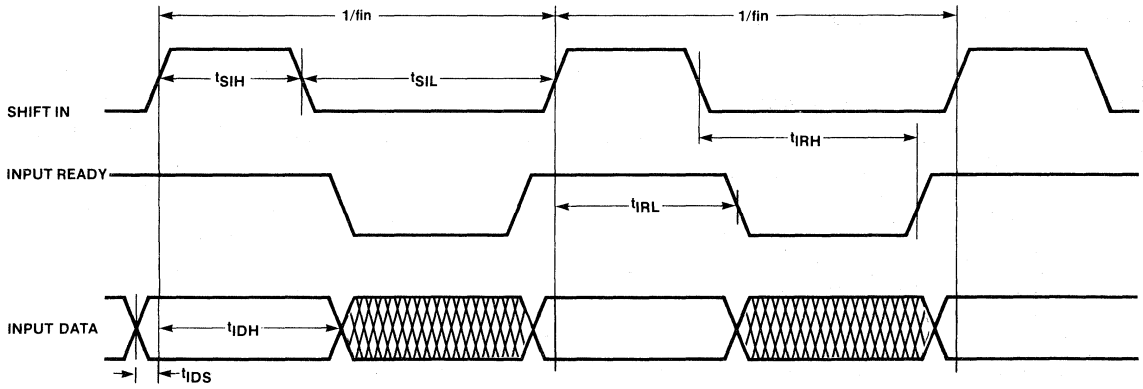


Figure 1. Input Timing

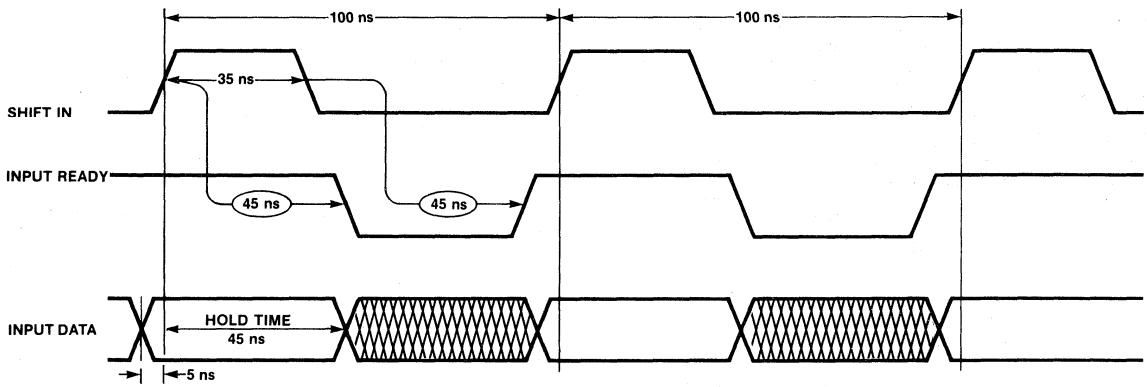


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate

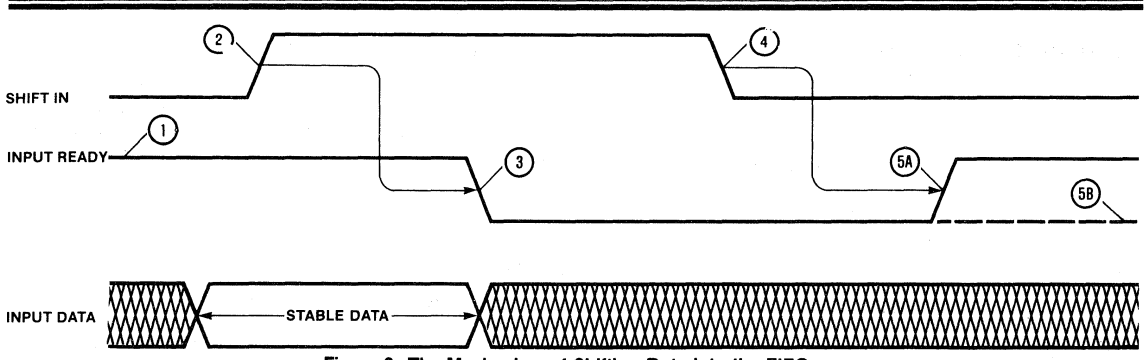


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

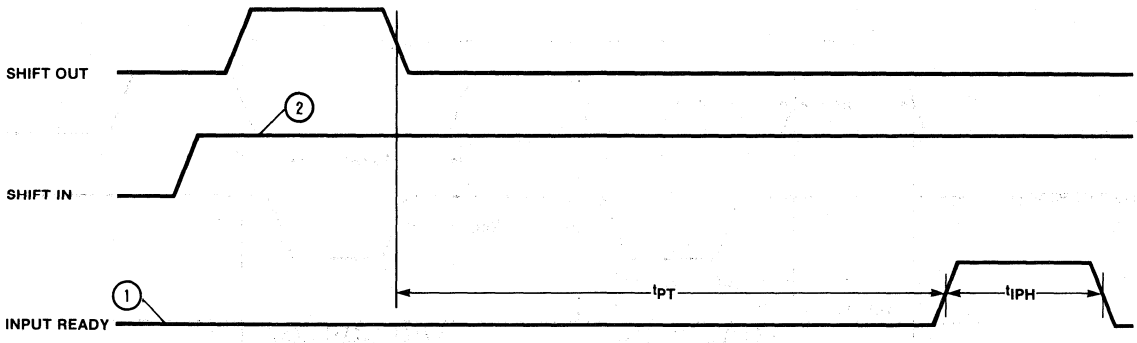


Figure 4. t_{IPH} Specification

(1) FIFO is initially full.
(2) Shift In held HIGH.

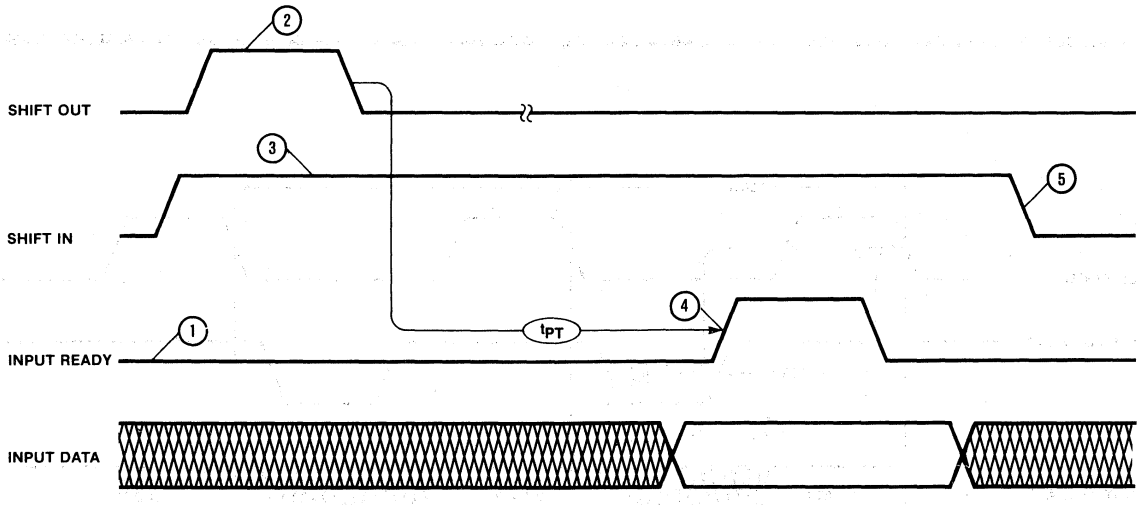


Figure 5. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location start "bubbling" to the front.
(3) Shift In is held HIGH.
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
(5) The Data from the first word is released for "fall through" to second word.

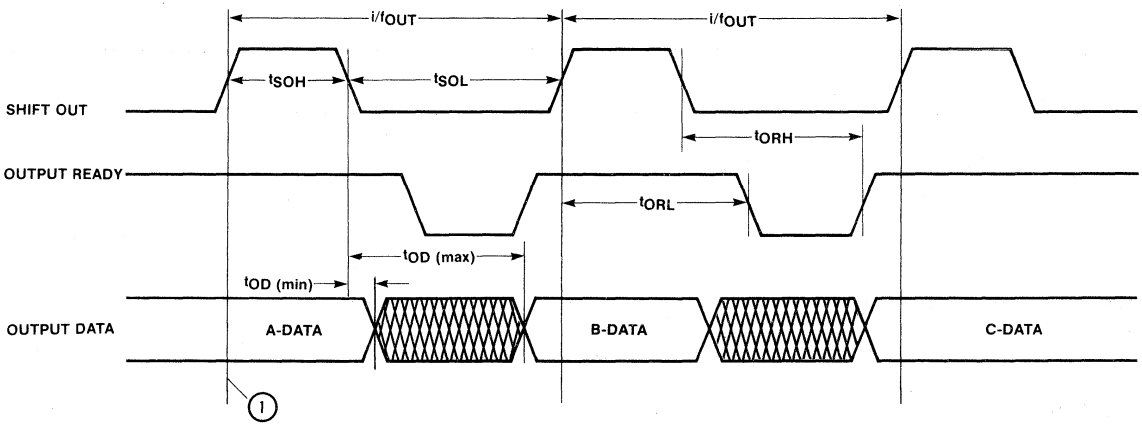


Figure 6. Output Timing

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

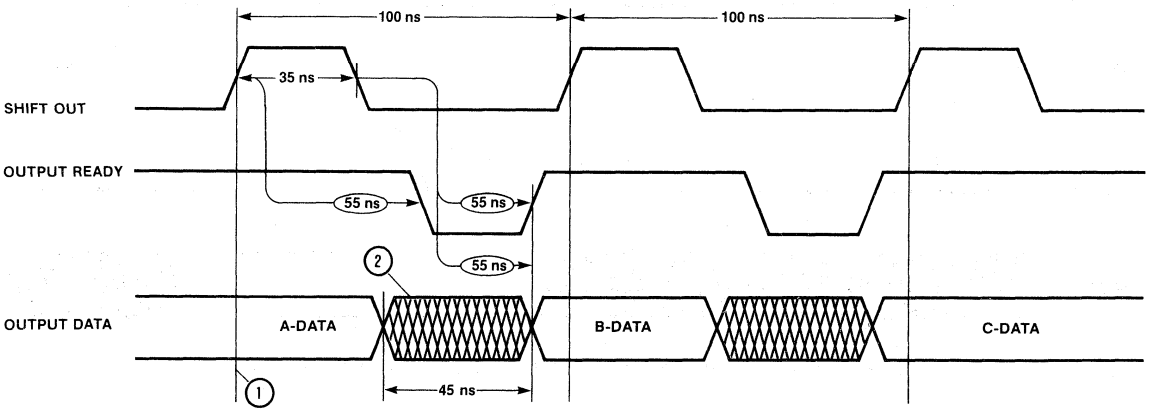


Figure 7. Typical Waveforms for 10 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

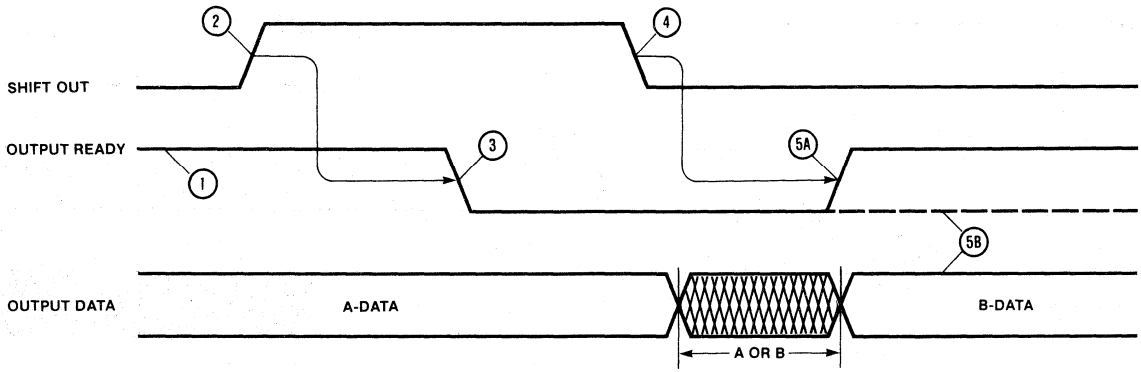


Figure 8. The Mechanism of Shifting Data Out of the FIFO.

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Input Ready stays LOW and the A-DATA remains unchanged at the outputs.

7

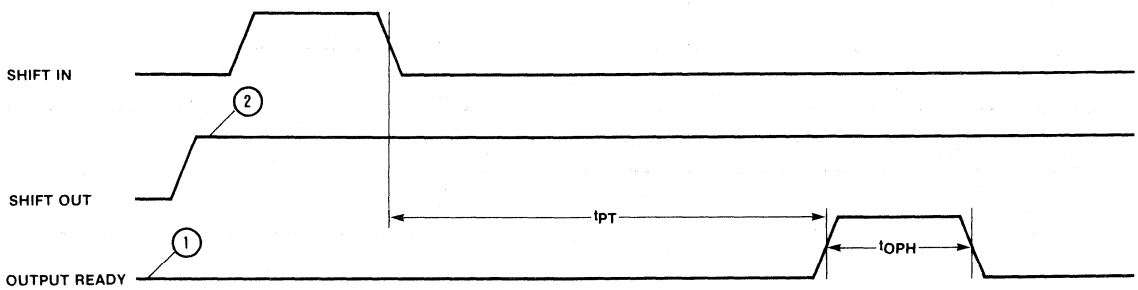


Figure 9. t_{PT} and t_{OPH} Specification

(1) FIFO initially empty.

(2) Shift Out held HIGH.

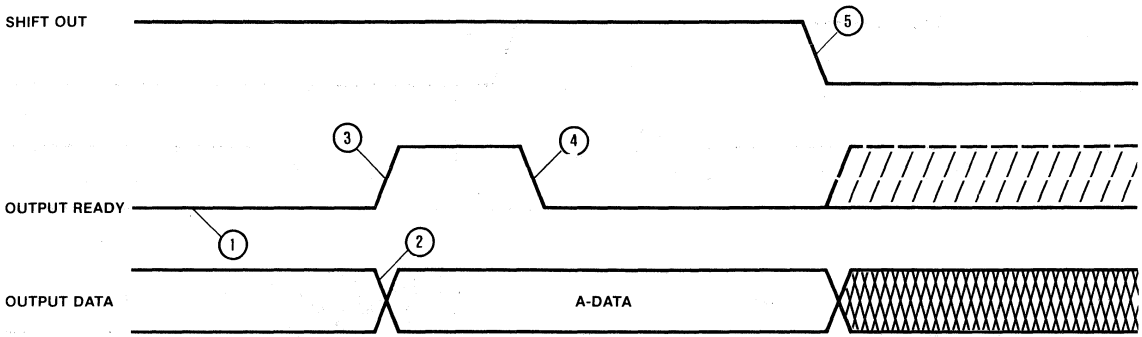


Figure 10. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

(1) Word 63 is empty.
(2) New data (A) arrives at the outputs (word 63).
(3) Output Ready goes HIGH indicating the arrival of the new data.
(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.
(5) As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.

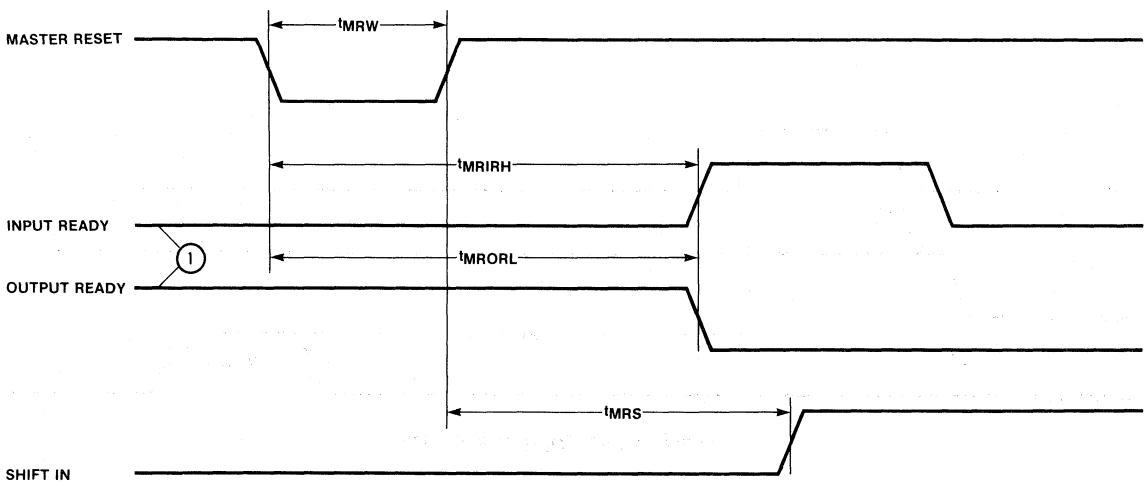


Figure 11. Master Reset Timing

(1) FIFO initially full.

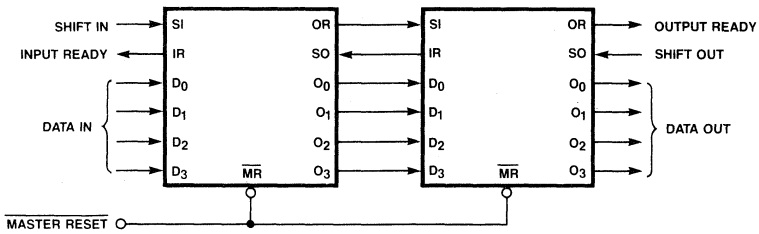


Figure 12. Cascading FIFOs to Form 128x4 FIFO.

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

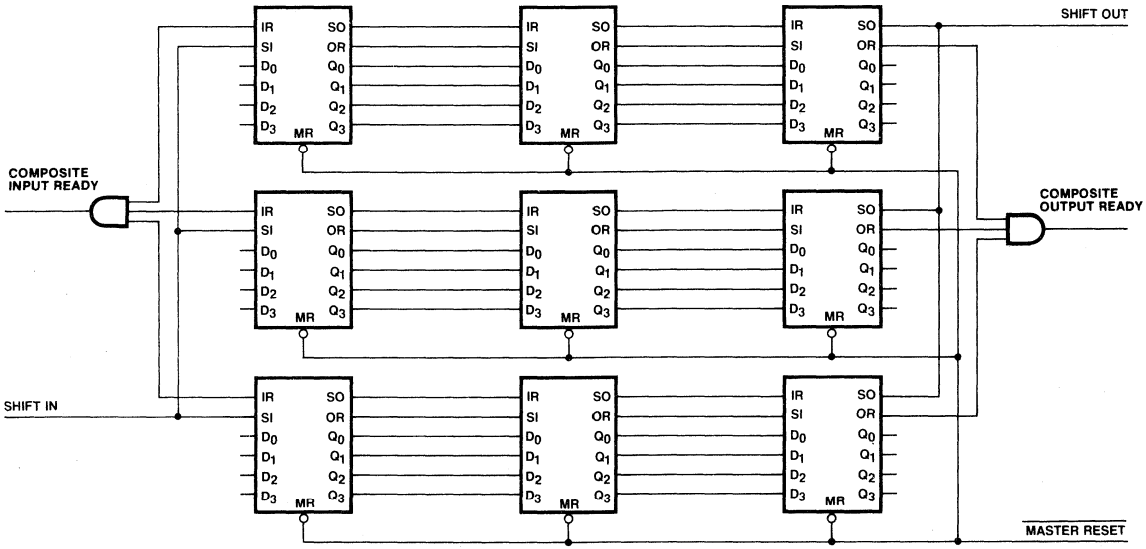
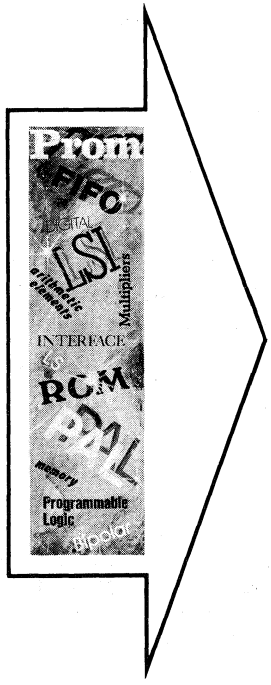


Figure 13. 192x12 FIFO.

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.



The following selection guides are designed to simplify the choice of the particular function to fit the specific application.

High Speed Parallel Multipliers

DESCRIPTION	PART NO.	MAX DELAY	PINS	PAGE
8x8 Multiplier	67558-1	125 ns	40	8-3
	57558-1	135 ns	40	
	67558	150 ns	40	
	57558	155 ns	40	
8x8 Pipelined multiplier	67559 †	65 ns	40	†
	57559 †			
16x16 Pipelined multiplier	MPY-16 †	140 ns	64	†

Sequential Multipliers/Accumulators/Dividers

DESCRIPTION	PART NO.	MULTIPLICATION TIME	PINS	PAGE
8 Bits	67508 †	400 ns	24	†
	57508 †			
16 Bits	67516 †	800 ns	24	†
	57516 †			

Look-Up Tables

DESCRIPTION	PART NO.	MAX ACCESS TIME	PINS	PAGE
Sine (0°-90°) Look-Up Table	6086/7	100 ns	24	8-9
	5086/7	150 ns	24	8-9

MSI Arithmetic Elements

DESCRIPTION	PART NO.	MAX. ADD TIME	MAX. CARRY (OR GENERATE) TIME	PINS	PAGE
4 Bit ALU	5/74S381	27 ns	20 ns	20	8-11
4 Bit fast ALU (pin compatible to 74S381)	5/67S581/2†	17 ns	15 ns	20	†
4 Group carry-look-ahead generator	5/74S182		7 ns	16	8-15

† Data Sheet will appear in a future edition of the LSI Data Book. The performance shown is a design goal. Contact Application Department for additional information.

8 x 8 Multiplier

57/67558 57/67558-1

U.S. Patent 4153938

Features/Benefits

- **Industry Standard**
- **Easy to Use; Combinatorial**
- **Unsigned, Signed, or Mixed Multiplication**
- **Rounding Inputs for Signed or Unsigned Operation**
- **Three-State Outputs for Bus Operation**
- **High Speed — 125 ns Max**

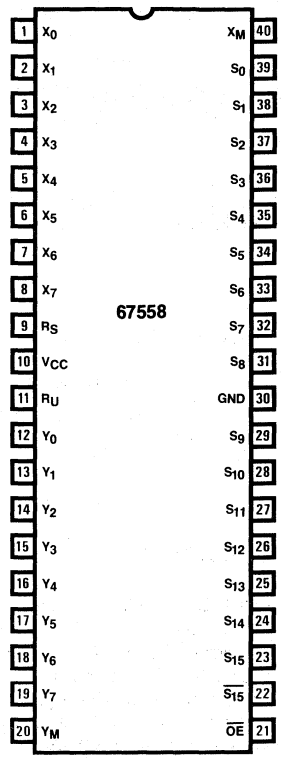
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
57558, 57558-1	J40	Military
67558, 67558-1	J40	Commercial

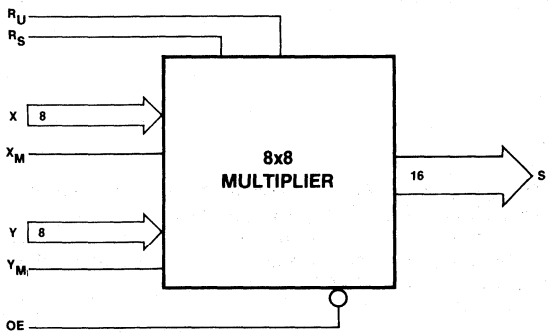
Description

The 57558/67558 is a high speed 8 x 8 combinatorial Multiplier which can multiply two eight-bit unsigned or signed 2s complement numbers and generate the sixteen-bit unsigned or signed product. Each input operand X and Y has an associated Mode control line, X_M and Y_M respectively. When a Mode control line is at a Low logic level the operand is treated as an unsigned eight-bit number while if the Mode control is at a High logic level the operand is treated as an eight-bit signed 2s complement number. Two additional inputs R_S and R_U allow the addition of a bit in the multiplier array at the appropriate bit positions for rounding signed or unsigned fractional numbers. The most significant product bit is available in both True and Complement form to assist in expansion to larger signed multipliers. The product outputs are three-state, controlled by an active Low Output Enable which allows several Multipliers to be connected to a parallel bus or be used in a pipelined system. The device uses a single +5V power supply and is packaged in a standard 40-pin DIP.

Pin Configuration



Logic Symbol



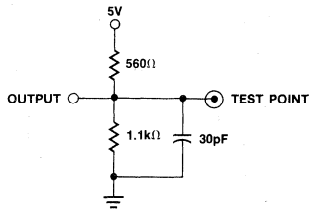
8

Switching Characteristics

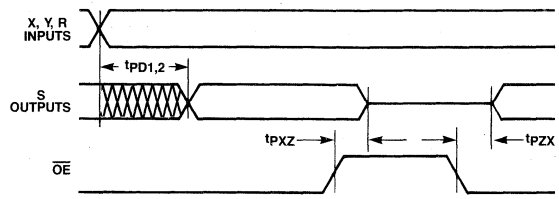
Over operating conditions

SYMBOL	PARAMETER	DEVICE	TYP	MAX	UNIT
t_{PXZ}	Delay from OE to S High Impedance State	67558 57558 67558-1 57558-1	30 30 30 30	40 50 40 50	ns
t_{PZX}	Delay from OE to S Active State	67558 57558 67558-1 57558-1	30 30 30 30	40 50 40 50	ns
t_{PD1}	Delay from Y, X to S_{0-4}	67558 57558 67558-1 57558-1	80 80 80 80	135 140 115 125	ns
t_{PD2}	Delay from Y, X to S_{5-15}, S_{15}	67558 57558 67558-1 57558-1	100 100 100 100	150 155 125 135	ns

Standard Test Load



Timing Waveform



Functional Description

The 57558/67558 Multiplier is an 8 x 8 combinatorial logic array capable of multiplying numbers in unsigned, signed 2s complement, or mixed notation. Each eight-bit input operand X and Y has associated with it a mode control which determines whether the array treats the number as signed or unsigned. If the mode control is at a High Logic level then the operand is treated as a 2s complement number with the most significant bit having a negative weight, while if the mode control is at a Low Logic level then the operand is treated as an unsigned number.

The multiplier provides all 16 product bits generated by the multiplication. For expansion during signed or mixed multiplication the most significant product bit has both true and complement available. This allows an adder to be used as a subtractor in many applications and eliminates the need for SSI circuits.

Two inputs, R_S and R_U, are additional inputs to the array which allow the addition of a bit at the appropriate positions in the array so as to provide rounding to the best signed or unsigned fractional eight-bit result. These inputs can also be used for rounding in larger multipliers.

The product outputs of the multiplier are controlled by an active Low Output Enable control. When this control is at a Low Logic level the multiplier outputs are active, while if the control is at a High Logic level then the outputs are placed in a high-impedance state. This three-state capability allows multipliers to be placed on a common bus and also allows pipelining of multiplications for higher speed systems.

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature				0		75	°C
T_C	Operating case temperature	–55		125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			–1	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			100	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = –2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V			–100	μA
I_{OZH}			V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0V	–10		–90	mA
I_{CC}	Supply current	V_{CC} = MAX			180	280	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

8

Rounding

Multiplication of two n-bit operands results in 2n-bit product†. Therefore, in n-bit system it is necessary to convert the double-length product into a single-length product. This can be accomplished by truncating or rounding. The following examples, illustrate the difference between the two conversion techniques in decimal arithmetic.

39.2 → 39
39.6 → 39
} Truncating

39.2 + 0.5 = 39.7 → 39
39.6 + 0.5 = 40.1 → 40
} Rounding

Obviously, rounding maintains more precision then truncating, but it may take one more step to implement. The additional step involves adding one-half of the weight of the single length LSB to the MSB of the discarded part e.g. in decimal arithmetic rounding 39.28 to one decimal point is accomplished by adding 0.05 to the number and truncating the LSB.

$$39.28 + 0.05 = 39.33 \rightarrow 39.3$$

The situation in binary arithmetic is quite similar, but two cases need to be considered; signed and unsigned data representation. In signed multiplication, the two MSBs are identical (except when both operands are −1) therefore, the best single length product is shifted one position to the right with respect to the unsigned multiplications. Figure 1 illustrates these two cases for the 8x8 multiplier. In the signed case, adding one-half of the S_7 weight is accomplished by adding 1 in bit position 6, and in the unsigned case 1 is added to bit position 7. Therefore, the 67558 multiplier has two rounding inputs, R_S and R_U. Thus, to get a rounded single length result the appropriate R input is tied to V_{CC} (logic one) and the other R input is grounded. If double length result is desired both R inputs are grounded.

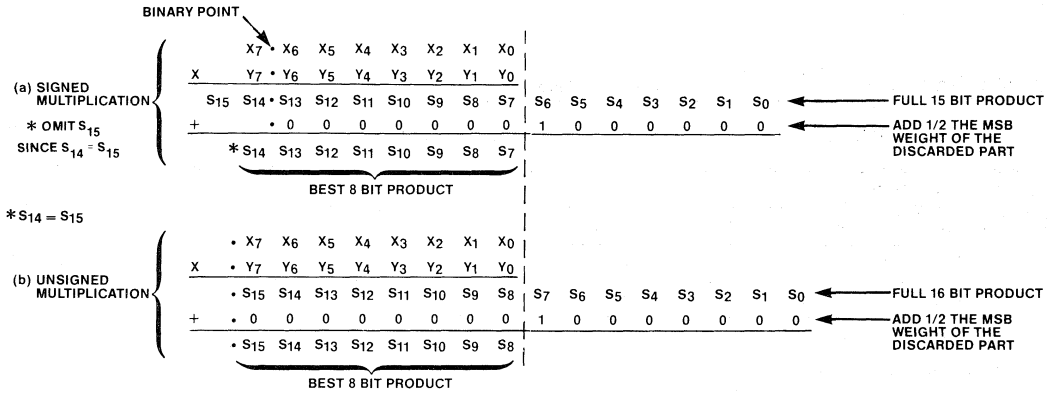


Figure 1. Rounding the Result of Binary Fractional Multiplication.

(a) In signed (2's complement) notation, the MSB of each operand is the sign bit, and the binary point is to the right of the MSB. The resulting product has a redundant sign bit and the binary point is to the right of the second MSB of the product. The best eight-bit product is from S_{14} through S_7, and rounding is performed by adding "1" to bit position S_6.
(b) In unsigned notation the best 8-bit product, is the most significant half of the product, corrected by adding "1" to bit position S_7.

† In general: multiplication of M-bit operand by N-bit operand results in M + N bit product.

Signed Expansion

The most significant product bit has both true and complement outputs available. When building larger signed multipliers the partial products except at the lower stages are signed numbers. These unsigned and signed partial products must be added together to give the correct signed product. Having both the true and complement of the most significant product bit available assists in this addition. For example, say that two signed partial products must be added and MSI adders are used; we then have the situation of adding together the Carry from the previous adder stage plus the addition of the two negative most significant partial product bits. The result of adding these variables must be a positive sum and a negative carry (borrow). The equations for this are:

$$S = A \oplus B \oplus C$$

$$C_0 = AB + BC + CA$$

where C is the Carry In and A and B the sign bits of the two partial products.

Now an adder produces the equations:

$$S = A \oplus B \oplus C$$

$$C_0 = AB + BC + CA$$

Examining these equations it can be seen that if the inversion of A and B are used then the adder produces the inversion of the negative carry since

$$AB + B\overline{C} + \overline{C}A = \overline{\overline{A}\overline{B}} + BC + C\overline{A},$$

and the sum remains the same.

16 x 16 Two's Complement Multiplication

The 16-bit X operand is broken into two 8-bit operands (X_0-X_7 and X_8-X_{15}), and so is the Y operand. Since the situation is that of a cross product, four partial products are generated as follows:

$$A = X_L * Y_L$$
$$B = X_L * Y_H$$
$$C = X_H * Y_L$$
$$D = X_H * Y_H$$

where the subscript L stands for bits 0-7, and the subscript H stands for bits 8-15.

Expanding in two's complement multiplication requires a sign extension of the B and C partial products. Thus, B_{15} and C_{15} need to be extended eight positions to the left (to align with D_{15}). In this approach two more adders are required. But the complement of the MSB (S_{15}) on the 67558 can be used to save these two adders. The Figure shows the implementation of such a 16x16 signed two's complement multiplication.

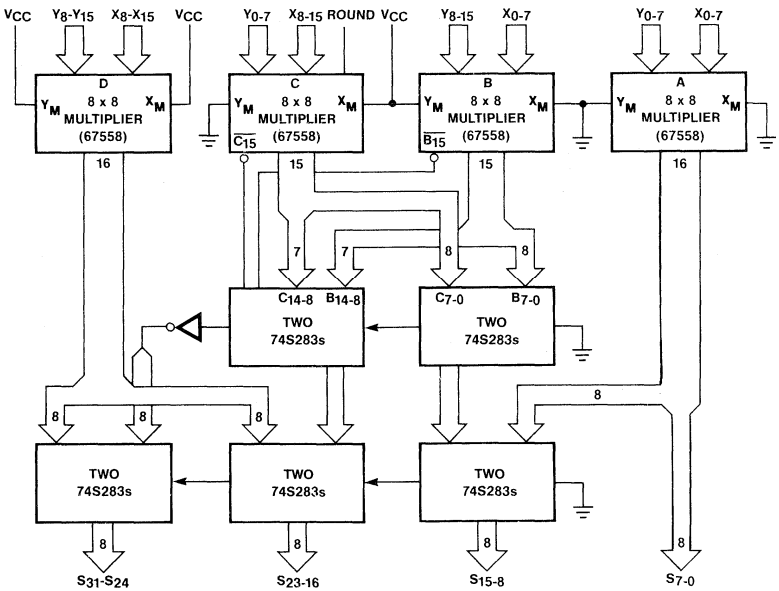


Figure 2. 16 x16 Two's Complement Signed Multiplication.

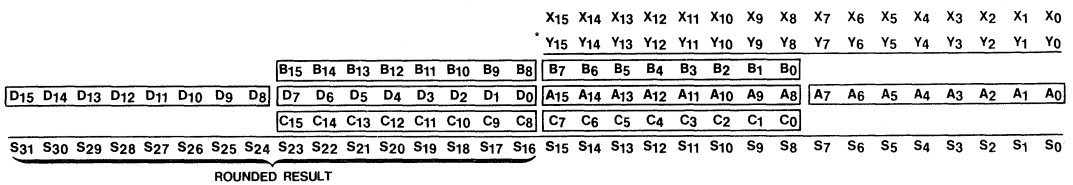


Figure 3. Unsigned Expansions of the 8x8 Multiplier to 16x16 Multiplication.

Sine (0° to 90°) Look Up Table Using a 1024 X 10 ROM (5/6255 5/6256) 5/6086 5/6087

Features/Benefits

- **Input angle increments of 90°/1024 = .0879°**
- **10 bit binary outputs**
- **Low power dissipation. Typically 500 mw**
- **Fast access time 100 ns max.**
- **TTL compatible**

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
5086/87	J24	Military
6086/87	J24	Commercial

Description

The 5255/6255, 1024 words by 10 bits Read Only Memory has been customized to make a sine θ look up table (5086/6086) for $0° \leq \theta < 90°$. The address inputs are used to divide the first 90° quadrant into angles increments of 90°/1024 words or .0879°/word. The memory outputs should be interpreted as binary weighted fractions where output 1 has a weight of 1/2 or .500, output 2 has a weight of 1/4 or .250, and so on until output 10 which has a weight of 1/1024 or .000976. The 10 bit output code has not been rounded off so that output error will always be positive and less than 1/1024 or .0009765. Round off error, in approximating the ROM input word, must be added or subtracted to the output error. For electrical characteristics and pin out refer to 6255 specifications (pages 4-3 through 4-5).

Example 1:

Find the sine 45°

Let X = the ROM word where sine 45° is stored

$$\frac{X}{1024 \text{ words}} = \frac{45°}{90°}$$

X = word 512

Word 511 has the following stored data and interpretation:

Output #	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	O_{10}	
Stored Data	H	L	H	H	L	H	L	H	L	L	(H = TTL HIGH)
Binary Weight	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256	1/512	1/1024	

Adding the fractions wherever an "H" appears given.

$$\frac{1}{2} + \frac{1}{8} + \frac{1}{16} + \frac{1}{64} + \frac{1}{256} = .50000 + .12500 + .06250 + .01562 + .00391 = .70507$$

Handbook Value = .70711

Our Error = .70711 − .70703 = .00008

Example 2:

Find the sine 210°

This value is in quadrant three, therefore, $\theta' = 210° - 180°$ or 30°

Let X = the ROM word where sine 30° is stored $\frac{X}{1024 \text{ words}} = \frac{30°}{90°}$

X = word 341.33 (round off to word 341)

Word 341 has the following stored data and interpretation:

Output #	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	O_{10}
Stored Data	L	H	H	H	H	H	H	H	H	H
Binary Weight	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256	1/512	1/1024

Adding the fractions wherever an "H" appears gives 0.49902

The sine 210°, therefore, = −.49902 with the sign generated by external logic. Note that the address 341 to which we rounded off is actually the sine 29.97°.

Arithmetic Logic Unit/ Function Generator

SN54S381 SN74S381

Features/Benefits

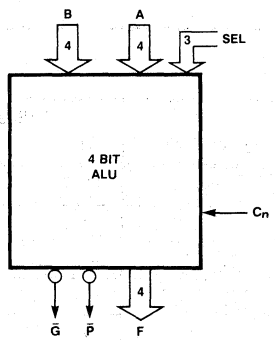
- **A Fully Parallel 4-Bit ALU in 20-Pin Package for 0.300-inch Row Spacing**
- **Ideally Suited for High-Density Economical Processors**
- **Parallel Inputs and Outputs and Full Look-Ahead Provide System Flexibility**
- **Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:**

  A Minus B
  B Minus A
  A Plus B
  and Five Other Functions

Description

The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A fully carry look-ahead circuit is provided for fast, simultaneous carry generation by means of two cascade outputs ($\overline{P}$ and $\overline{G}$) for the four bits in the package.

Logic Symbol

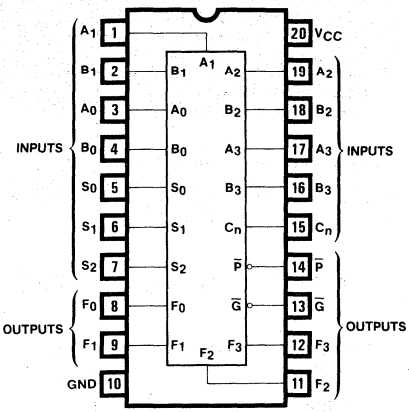


Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S381	J20	Military
SN74S381	J20	Commercial

Pin Configuration

SN54S381, SN74S381



Function Table

SELECTION			ARITHMETIC/LOGIC OPERATION
S2	S1	S0	
L	L	L	Clear †
L	L	H	B minus A
L	H	L	A minus B
L	H	H	A plus B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	Preset ††

† Force all F outputs to be Lows.
†† Force all F outputs to be Highs.

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Storage Temperature Range ..... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		70	°C

Electrical Characteristics Over operating conditions

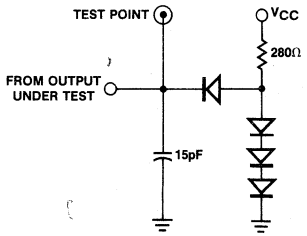
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN I_I = −18mA				−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX V_I = 0.5V	Any S input			−2	mA
			Cn			−8	
			All others			−6	
I_{IH}	High-level input current	V_{CC} = MAX V_I = 2.7V	Any S input			50	μA
			Cn			250	
			All others			200	
I_I	Maximum input current	V_{CC} = MAX V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OL} = 20mA				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OH} = −1mA	SN54S381	2.4	3.4		V
			SN74S381	2.7	3.4		
I_{OS}	Output short-circuit current*	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX			105	160	mA

* Not more than one output should be shorted at a time.

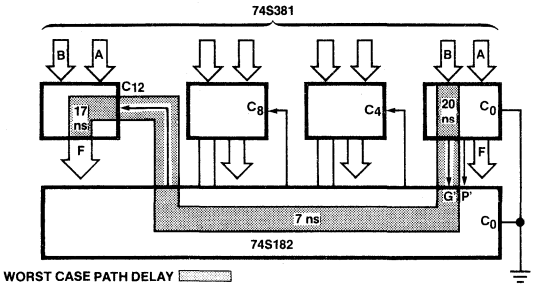
Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	5/74S381 TYP	5/74S381 MAX	UNIT
t_P	Propagation delay time	C_n	Any F	10	17	ns
t_P	Propagation delay time	Any A or B	$\overline{G}$	12	20	ns
t_P	Propagation delay time	Any A or B	$\overline{P}$	11	18	ns
t_{PLH}	Propagation delay, low-to-high	Ai or Bi	Fi	18	27	ns
t_{PHL}	Propagation delay, high-to-low			16	25	ns
t_P	Propagation delay time	Any S	Fi, $\overline{G}$, $\overline{P}$	18	30	ns

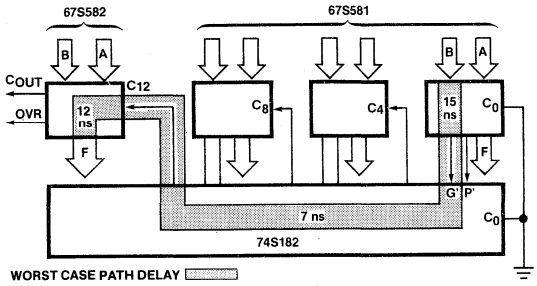
Standard Test Load



16-BIT ALU (USING 74S381)



16-BIT ALU (USING 67S581/2)



MAXIMUM DELAY OF ADDITION/SUBTRACTION.

	74S381	67S581
1-4 bits	27ns	22ns
5-16 bits	44ns	34ns
17-64 bits	64ns	54ns

8

Look-Ahead Carry Generators

SN54S182 SN74S182

Description

The SN54S182, and SN74S182 are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table below.

When used in conjunction with 74S381, 67S581, 74S181, 2901, 6701 arithmetic logic units (ALU), these generators provide high-speed carry lookahead capability for any word length. Each 'S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits.

The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Logic equations for the 'S182 are:

$$C_{n+x} = G0 + P0\ Cn$$

$$C_{n+y} = G1 + P1\ G0 + P1\ P0\ Cn$$

$$C_{n+z} = G2 + P2\ G1 + P2\ P1\ G0 + P2\ P1\ P0\ Cn$$

$$\overline{G} = \overline{G3 + P3\ G2 + P3\ P2\ G1 + P3\ P2\ P1\ G0}$$

$$\overline{P} = \overline{P3\ P2\ P1\ P0}$$

or

$$\overline{C}_{n+x} = \overline{Y0\ (X0 + Cn)}$$

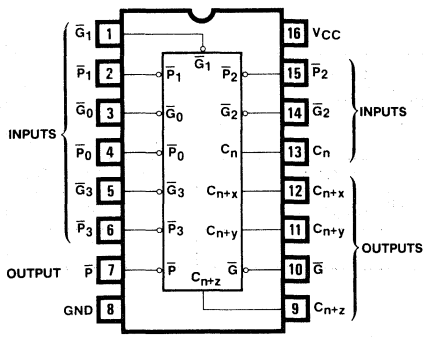
$$\overline{C}_{n+y} = \overline{Y1\ [X1 + Y0\ (X0 + Cn)]}$$

$$\overline{C}_{n+z} = \overline{Y2\ \{X2 + Y1\ [X1 + Y0\ (X0 + Cn)]\}}$$

$$Y = Y3\ (X3 + Y2)\ (X3 + X2 + Y1)\ (X3 + X2 + X1 + Y0)$$

$$X = X3 + X2 + X1 + X0$$

Pin Configuration



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S182	J16	Military
SN74S182	J16	Commercial

Summarizing Tables

FUNCTION TABLE FOR C_{n+y} OUTPUT

INPUTS $\overline{G}1$ $\overline{G}0$ $\overline{P}1$ $\overline{P}0$ C_n	OUTPUT C_{n+y}
L X X X X	H
X L L X X	H
X X L L H	H
All other combinations	L

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS $\overline{P}3$ $\overline{P}2$ $\overline{P}1$ $\overline{P}0$	OUTPUT $\overline{P}$
L L L L	L
All other combinations	H

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS $\overline{G}0$ $\overline{P}0$ C_n	OUTPUT C_{n+x}
L X X	H
X L H	H
All other combinations	L

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS $\overline{G}3$ $\overline{G}2$ $\overline{G}1$ $\overline{G}0$ $\overline{P}3$ $\overline{P}2$ $\overline{P}1$	OUTPUT $\overline{G}$
L X X X X X X	L
X L X X L X X	L
X X L X L L X	L
X X X L L L L	L
All other combinations	H

FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS $\overline{G}2$ $\overline{G}1$ $\overline{G}0$ $\overline{P}2$ $\overline{P}1$ $\overline{P}0$ $\overline{C}_n$	OUTPUT C_{n+z}
L X X X X X X	H
X L X L X X X	H
X X L L L X X	H
X X X L L L H	H
All other combinations	L

H = High Level, L = Low Level, X = Irrelevant. Any inputs not shown in a given table are irrelevant with respect to that output.

8

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Storage Temperature Range ..... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		70	°C

Electrical Characteristics Over operating conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN, I_I = −18mA				−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V	C_n input			−2	mA
			$\overline{P}_3$ input			−4	
			$\overline{P}_2$ input			−6	
			$\overline{P}_0$, $\overline{P}_1$, or $\overline{G}_3$ input			−8	
			$\overline{G}_0$ or $\overline{G}_2$			−14	
			$\overline{G}_1$ input			−16	
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V	C_n input			50	μA
			$\overline{P}_3$ input			100	
			$\overline{P}_2$ input			150	
			$\overline{P}_0$, $\overline{P}_1$, or $\overline{G}_3$ input			200	
			$\overline{G}_0$ or $\overline{G}_2$			350	
			$\overline{G}_1$ input			400	
I_I	Maximum input current	V_{CC} = MAX, V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −1mA				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20mA	SN74S182	2.7	3.4		V
			SN54S182	2.5	3.4		
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−40		−100	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX, See Note 1	SN74S182		69	109	mA
			SN54S182		69	99	
I_{CCH}	Supply current, all outputs high	V_{CC} = 5V, See Note 2			35		mA

*Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

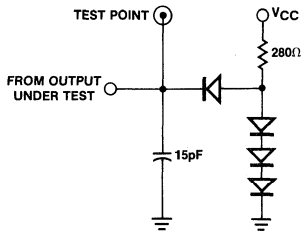
NOTES: 1. ICCL is measured with all outputs open; inputs $\overline{G}0$, $\overline{G}1$, and $\overline{G}2$ at 4.5 V; and all other inputs grounded.

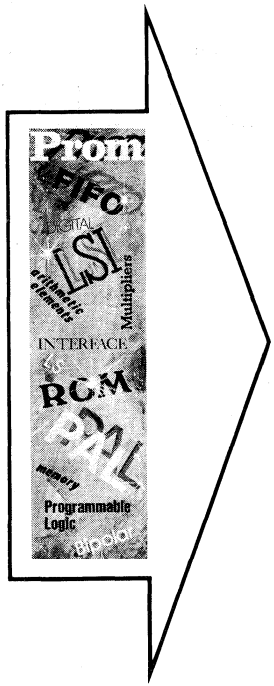
2. ICCH is measured with all outputs open, inputs $\overline{P}3$ and $\overline{G}3$ at 4.5 V, and all other inputs grounded.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high	$\overline{G}0$, $\overline{G}1$, $\overline{G}2$, $\overline{G}3$,	C_{n+x}, C_{n+y},	4.5	7	ns
t_{PHL}	Propagation delay, high-to-low	$\overline{P}0$, $\overline{P}1$, $\overline{P}2$, or $\overline{P}3$	or C_{n+z}	4.5	7	ns
t_{PLH}	Propagation delay, low-to-high	$\overline{G}0$, $\overline{G}1$, $\overline{G}2$, $\overline{G}3$,	$\overline{G}$	5	7.5	ns
t_{PHL}	Propagation delay, high-to-low	$\overline{P}1$, $\overline{P}2$, or $\overline{P}3$		7	10.5	ns
t_{PLH}	Propagation delay, low-to-high	$\overline{P}0$, $\overline{P}1$, $\overline{P}2$, or $\overline{P}3$	$\overline{P}$	4.5	6.5	ns
t_{PHL}	Propagation delay, high-to-low			6.5	10	ns
t_{PLH}	Propagation delay, low-to-high	C_n	C_{n+x}, C_{n+y},	6.5	10	ns
t_{PHL}	Propagation delay, high-to-low		or C_{n+z}	7	10.5	ns

Standard Test Load





Octal Interface Selection Guide

FUNCTION	POWER	POLARITY	FEATURE	PART NUMBER		PAGE
				COMMERCIAL	MILITARY	
Buffer	LS	Non-invert	—	SN74LS244	SN54LS244	3
			—	SN74LS241	SN54LS241	3
			Schmitt Trigger	67LS304	57LS304	6
			Schmitt Trigger	67LS301	57LS301	6
		Invert	—	SN74LS240	SN54LS240	3
			Schmitt Trigger	67LS300	57LS300	6
	S	Non-invert	—	SN74S244	SN54S244	3
			—	SN74S241	SN54S241	3
		Invert	—	SN74S240	SN54S240	3
Transceiver	LS	Non-invert	—	SN74LS645	SN54LS645	8
Latch	LS	Non-invert	—	SN74LS373	SN54LS373	10
		Invert	—	67LS380	57LS380	13
	S	Non-invert	—	SN74S373	SN54S373	10
			32mA I_{OL}	67S373	—	16
		Invert	—	67S380	57S380	13
			32mA I_{OL}	67S382	—	18
Register	LS	Non-invert	—	SN74LS374	SN54LS374	10
		Invert	—	67LS376	57LS376	13
	S	Non-invert	—	SN74S374	SN54S374	10
			32mA I_{OL}	67S374	—	16
		Invert	—	67S376	57S376	13
			32mA I_{OL}	67S378	—	18

Package Types — All octal interface are in the 20 pin dual-in-line ceramic or plastic package.

Octal Buffers

SN54/74LS240 SN54/74S240
SN54/74LS241 SN54/74S241
SN54/74LS244 SN54/74S244

Features/Benefits

- **Three-state outputs drive bus lines**
- **Low current PNP inputs reduce loading**
- **20-pin Skinny DIP™ saves space**
- **8-bits matches byte boundaries**
- **Ideal for microprocessor interface**

Description

The Octal Buffers provide high speed and high current interface capability for bus organized Digital Systems. The three-state drivers will source a termination to ground (up to 133Ω) or sink a pull-up to V_{CC} as in the popular 220Ω/330Ω computer peripherial termination. The PNP inputs provide improved fan-in with 0.2 mA I_{IL} on the Low Power Schottky buffers and 0.4mA I_{IL} on the Schottky buffers.

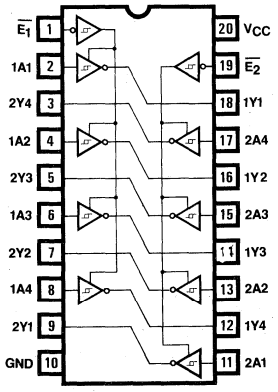
The 240 and 244 provide inverting and non-inverting outputs with active low enables. The 241 provides non-inverting outputs with both active low and active high enables allowing transceiver operation.

Ordering Information

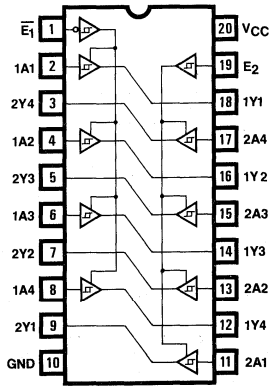
PART NUMBER	PKG	TEMP.	ENABLE	POLARITY	POWER
SN54LS240 SN74LS240	J N,J,	mil com	LOW	Invert	LS
SN54LS244 SN74LS244	J N,J	mil com	LOW	Non-invert	
SN54LS241 SN74LS241	J N,J	mil com	HIGH-LOW		
SN54S240 SN74S240	J N,J	mil com	LOW	Invert	S
SN54S244 SN74S244	J N,J	mil com	LOW	Non-Invert	
SN54S241 SN74S241	J N,J	mil com	HIGH-LOW		

Logic Symbols

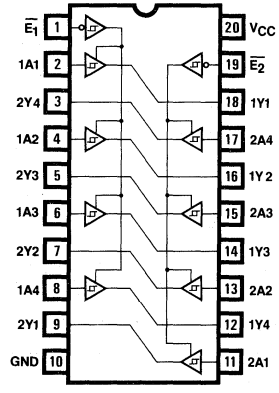
240 Octal Buffer



241 Octal Buffer



244 Octal Buffer



™Skinny DIP is a trademark of Monolithic Memories

Absolute Maximum Ratings

Supply Voltage V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN,	I_I = −18mA			−1.5			−1.5	V
ΔV_T	Hysteresis ($V_{T_+} - V_{T_-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4V			−0.2			−0.2	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7V			20			20	μA
I_I	Maximum input current		V_{CC} = MAX,	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA			0.4			0.4	V
				I_{OL} = 24mA						0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.5V, V_{IH} = 2V	I_{OH} = −3mA	2.4	3.4		2.4	3.4		V
				I_{OH} = −12mA	2						
				I_{OH} = −15mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			−20			−20	μA
I_{OZH}				V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	LS240		17	27		17	27	mA
				LS241, LS244		17	27		17	27	
		Outputs Low		LS240		26	44		26	44	
				LS241, LS244		27	46		27	46	
		Outputs Disabled		LS240		29	50		29	50	
				LS241, LS244		32	54		32	54	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS240			LS241, LS244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		9	14		12	18	ns
t_{PHL}				12	18		12	18	ns
t_{PZL}	Output Enable delay			20	30		20	30	ns
t_{PZH}				15	23		15	23	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		15	25	ns
t_{PHZ}				10	18		10	18	ns

Absolute Maximum Ratings

Supply Voltage V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125*	0		75	°C

*The SN54S241/244J operating at free air temperature above 116°C requires a heat sink such that $R_{\theta CA}$ is not more than 40°C/W.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.2			−1.2	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
I_{IL}	Low-level input current	Any A	V_{CC} = MAX	V_I = 0.5V			−0.4			−0.4	mA
		Any E					−2			−2	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 48mA			0.55				V
				I_{OL} = 64mA						0.55	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −1mA				2.7			V
				I_{OH} = −3mA	2.4	3.4		2.4	3.4		
				I_{OH} = −12mA	2						
				I_{OH} = −15mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50			−50	μA
I_{OZH}				V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current †		V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	S240		80	123		80	135	mA
				S241, S244		95	147		95	160	
		Outputs Low		S240		100	145		100	150	
				S241, S244		120	170		120	180	
		Outputs Disabled		S240		100	145		100	150	
				S241, S244		120	170		120	180	

†Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S240			S241, S244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to Output delay	C_L = 50pF R_L = 90Ω		4.5	7		6	9	ns
t_{PHL}				4.5	7		6	9	ns
t_{PZL}	Output Enable delay			10	15		10	15	ns
t_{PZH}				6.5	10		8	12	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 90Ω		10	15		10	15	ns
t_{PHZ}				6	9		6	9	ns

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Octal Buffers with Schmitt Triggers

57/67LS300 57LS301 57/67LS304

Features/Benefits

- Schmitt trigger guarantees high noise margin
- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- 20-pin Skinny DIP™ saves space
- 8-bits matches byte boundaries
- Ideal for microprocessor interface

Ordering Information

PART NUMBER	PKG	TEMP.	ENABLE	POLARITY	POWER
57LS300	J	mil	LOW	Invert	LS
67LS300	N,J	com			
57LS304	J	mil	LOW	Non-invert	
67LS304	N,J	com			
57LS301	J	mil	HIGH-LOW		
67LS301	N,J	com			

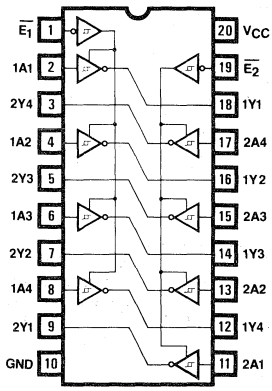
Description

In addition to the standard Schottky and Low Power Schottky Octal Buffers, Monolithic Memories provides a full hysteresis with "a true" Schmitt trigger circuit. The improved performance characteristics are designed to be consistent with the SN54/74LS14 Hex Schmitt trigger and guarantee a full 400 mV noise immunity. The Schmitt trigger operation makes the LS buffers ideal for bus receivers in a noisy environment.

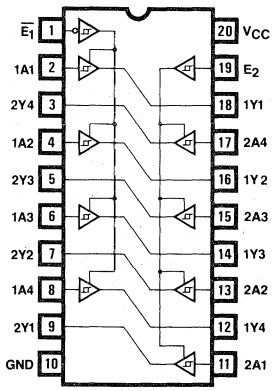
The Octal Buffers provide high speed and high current interface capability for bus organized Digital Systems. The PNP inputs provide improved fan-in with 0.2 mA I_{IL}. The 300 and 304 provide inverting and non-inverting outputs with active low enables. The 301 provides non-inverting outputs with both active low and active high enables allowing transceiver operation.

Logic Symbols

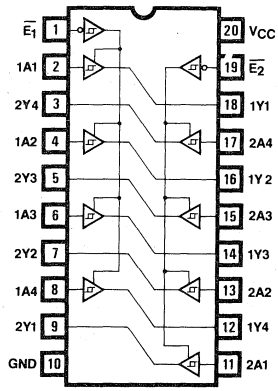
300 Octal Buffer



301 Octal Buffer



304 Octal Buffer



Absolute Maximum Ratings

Supply Voltage V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+}	Positive threshold voltage		V_{CC} = 5V		1.5	1.7	2.0	1.5	1.7	2.0	V
V_{T-}	Negative threshold voltage		V_{CC} = 5V		0.6	0.9	1.1	0.6	0.9	1.1	V
V_{IC}	Input clamp voltage		V_{CC} = MIN,	I_I = –18mA			–1.5			–1.5	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = 5V		0.4	0.8		0.4	0.8		V
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4V			–0.2			–0.2	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7V			20			20	μA
I_I	Maximum input current		V_{CC} = MAX,	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{T+} = 2V, V_{T-} = 0.6V	I_{OL} = 12mA			0.4			0.4	V
				I_{OL} = 24mA						0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{T+} = 2V, V_{T-} = 0.6V	I_{OH} = –3mA	2.4	3.4		2.4	3.4		V
				I_{OH} = –12mA	2						
				I_{OH} = –15mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{T+} = 2V, V_{T-} = 0.6V	V_O = 0.4V			–20			–20	μA
I_{OZH}				V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *		V_{CC} = MAX		–40		–225	–40		–225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open	LS300		17	27		17	27	mA
				LS301, LS304		18	31		18	31	
		Outputs Low		LS300		26	44		26	44	
				LS301, LS304		32	46		32	46	
		Outputs Disabled		LS300		29	50		29	50	
				LS301, LS304		34	54		34	54	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS300			LS301, LS304			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		19			19		ns
t_{PHL}				19			19		ns
t_{PZL}	Output Enable delay			37			26		ns
t_{PZH}				26			26		ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		19			22		ns
t_{PHZ}				19			22		ns

9

Octal Transceiver
SN54/74LS645

Features/Benefits

- **3-state outputs drive bus lines**
- **Low current PNP inputs reduce loading**
- **20 pin Skinny DIP™ saves space**
- **8-bits matches byte boundaries**
- **Ideal for microprocessor interface**

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS645	J	mil	Non-invert	LS
SN74LS645	N,J	com		

Description

These Octal Bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

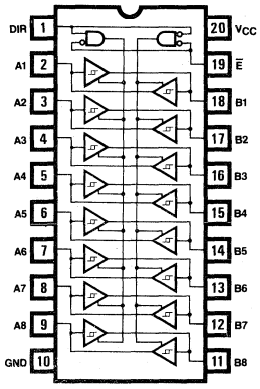
The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input (E) can be used to disable the device so that the buses are effectively isolated.

Function Table

ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolated

Logic Symbol

645 Octal Transceiver



Absolute Maximum Ratings

Supply Voltage V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN,	I_I = −18mA			−1.5			−1.5	V
ΔV_T	Hysteresis $(V_{T_+} - V_{T_-})$ A or B		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4V			−0.4			−0.4	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7V			20			20	μA
I_I	Maximum input current		V_{CC} = MAX,	V_I = 5.5V			0.1			0.1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −3mA	2.4	3.4		2.4	3.4		V
				I_{OH} = −12mA	2						
				I_{OH} = −15mA				2			
I_{OZL}	Off-state output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			−400			−400	μA
I_{OZH}				V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply Current	Outputs High	V_{CC} = MAX, Outputs open			48	70		48	70	mA
		Outputs Low				62	90		62	90	
		Outputs Disabled				64	95		64	95	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	A to B			B to A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data to Output delay	C_L = 45pF R_L = 667Ω		8	15		8	15	ns
t_{PHL}				11	15		11	15	ns
t_{PZL}	Output Enable delay			31	40		31	40	ns
t_{PZH}				26	40		26	40	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		15	25	ns
t_{PHZ}				15	25		15	25	ns

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Octal Latches, Octal Registers

SN54/74LS373 SN54/74S373
SN54/74LS374 SN54/74S374

Features/Benefits

- 3-State Outputs Drive Bus Lines
- 20 Pin Skinny DIP™ Saves Space
- 8 Bits Matches Byte Boundaries
- Hysteresis Improves Noise Margin
- Low Current PNP Inputs Reduce Loading
- Ideal for Microprocessor Interface

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN54LS373 SN74LS373	J N,J	mil com	Non-invert	Latch	LS
SN54LS374 SN74LS374	J N,J	mil com		Register	
SN54S373 SN74S373	J N,J	mil com		Latch	S
SN54S374 SN74S374	J N,J	mil com		Register	

Description

The latch passes eight (octal) bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight (octal) bits of input data and passes it to the output on the "rising edge" of the clock.

The three state outputs are active when $\overline{OE}$ is low, and high impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the octal devices are packaged in the popular 20 Pin Skinny DIP.™

Function Tables

373 Octal Latch

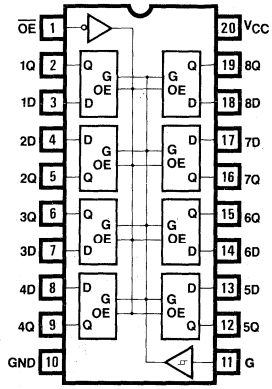
$\overline{OE}$	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

374 Octal Register

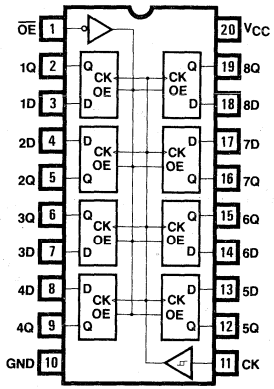
$\overline{OE}$	CK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Logic Symbols

373 Octal Latch



374 Octal Register



Monolithic Memories

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.5			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			−0.4			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			20			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA					0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −1mA	2.4	3.4					V
			I_{OH} = −2.6mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V			−20			−20	μA
I_{OZH}			V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	LS373		24	40		24	40	mA
			LS374		27	40		27	40	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS373 MIN	LS373 TYP	LS373 MAX	LS374 MIN	LS374 TYP	LS374 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 45pF R_L = 667Ω				35	50		MHz
t_{PLH}	Data to Output delay			12	18				ns
t_{PHL}				12	18				ns
t_{PLH}	Clock/Enable to output delay			20	30		15	28	ns
t_{PHL}				18	30		19	28	ns
t_{PZL}	Output Enable delay			25	36		21	28	ns
t_{PZH}				15	28		20	28	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		15	25		14	25	ns
t_{PHZ}				12	20		12	20	ns
t_w	Width of Clock/Gate	High	15			15			ns
		Low	15			15			
t_{su}	Setup time		0↓			20↑			ns
t_h	Hold time		10↓			0↑			

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Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			−0.25			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 20mA			0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2mA	2.4	3.4					V
			I_{OH} = −6.5mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50			−50	μA
I_{OZH}			V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S373		105	160		105	160	mA
			S374		90	140		90	140	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S373 MIN	S373 TYP	S373 MAX	S374 MIN	S374 TYP	S374 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			5	9				ns
t_{PHL}				9	13				ns
t_{PLH}	Clock/Enable to output delay			7	14		8	15	ns
t_{PHL}				12	18		11	17	ns
t_{PZL}	Output Enable delay			11	18		11	18	ns
t_{PZH}				8	15		8	15	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	12		7	12	ns
t_{PHZ}				6	9		5	9	ns
t_w	Width of Clock/Gate	High	6			6			ns
		Low	7.3			7.3			
t_{su}	Setup time		0↓			5↑			ns
t_h	Hold time		10↓			2↑			

Octal Latches, Octal Registers With Inverting Outputs

57/67LS376 57/67S376
57/67LS380 57/67S380

Features/Benefits

- Inverting Outputs
- 3-State Outputs Drive Bus Lines
- 20 Pin Skinny DIP™ Saves Space
- 8 Bits Matches Byte Boundaries
- Hysteresis Improves Noise Margin
- Low Current PNP Inputs Reduce Loading
- Ideal for Microprocessor Interface

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
57LS380 67LS380	J N,J	mil com	Invert	Latch	LS
57LS376 67LS376	J N,J	mil com		Register	
57S380 67S380	J N,J	mil com		Latch	S
57S376 67S376	J N,J	mil com		Register	

Description

In addition to the standard S and LS latches and Registers, Monolithic Memories provides inverting outputs instead of non-inverting outputs. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-Bit Slice to an active low bus.

The latch passes eight (octal) bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight (octal) bits of input data and passes it to the output on the "rising edge" of the clock.

The three state outputs are active when $\overline{OE}$ is low, and high impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the octal devices are packaged in the popular 20 Pin Skinny DIP.™

Function Tables

380 Octal Latch (Inverting)

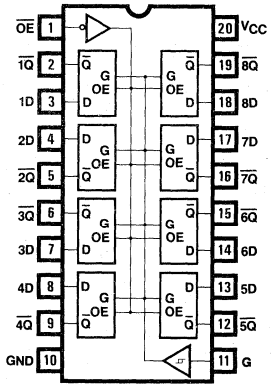
$\overline{OE}$	G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

376 Octal Latch (Inverting)

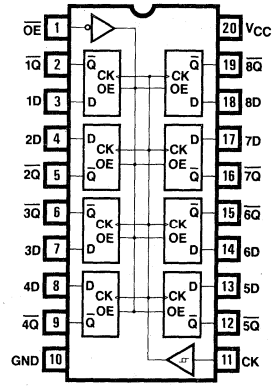
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

Logic Symbols

380 Octal Latch (Inverting)



376 Octal Register (Inverting)



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Monolithic Memories AMD

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA			-1.5			-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			-0.4			-0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			20			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7V			0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA		35	50		0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = -1mA	2.4	3.4					V
			I_{OH} = -2.6mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4V						-20	μA
I_{OZH}			V_O = 2.7V			20			20	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		-30		-130	-30		-130	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	LS 380		36	48		36	48	mA
			LS376		27	48		27	48	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	LS380			LS376			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum Clock frequency	C_L = 45pF R_L = 667Ω							MHz
t_{PLH}	Data to Output delay			17	25				ns
t_{PHL}				12	25				ns
t_{PLH}	Clock/Enable to output delay			20	35		19	30	ns
t_{PHL}				18	35		15	30	ns
t_{PZL}	Output Enable delay			25	36		21	30	ns
t_{PZH}				17	30		20	30	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		18	29		18	29	ns
t_{PHZ}				16	24		16	24	ns
t_w	Width of Clock/Gate	High	15			15			ns
		Low	15						
t_{su}	Setup Time		0↓			20↑			ns
t_h	Hold Time		10↓			0↑			

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.2			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5V			−0.25			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			50			50	μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 20mA			0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2mA	2.4	3.4					V
			I_{OH} = −6.5mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50			−50	μA
I_{OZH}			V_O = 2.4V			50			50	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S380		105	160		105	160	mA
			S376		90	140		90	140	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S380 MIN	S380 TYP	S380 MAX	S376 MIN	S376 TYP	S376 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			9	18				ns
t_{PHL}				5	16				ns
t_{PLH}	Clock/Enable to output delay			12	22		11	20	ns
t_{PHL}				7	20		8	18	ns
t_{PZL}	Output Enable delay			11	20		11	20	ns
t_{PZH}				8	17		8	17	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	16		7	16	ns
t_{PHZ}				6	13		5	13	ns
t_w	Width of Clock/Gate	High	6			6			ns
		Low	7.3			7.3			
t_{su}	Setup time		0↓			5↑			ns
t_h	Hold time		10↓			2↑			

Octal Latches, Octal Registers With 32mA Outputs

67S373 67S374

Features/Benefits

- 32mA I_{OL}
- 3-State Outputs Drive Bus Lines
- 20 Pin Skinny DIP™ Saves Space
- 8 Bits Matches Byte Boundaries
- Hysteresis Improves Noise Margin
- Low Current PNP Inputs Reduce Loading
- Ideal for Microprocessor Interface

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA.

The higher I_{OL} is intended for upgrading systems which presently satisfy 32 mA requirements with SN54/74365, 366, 367, 368, Hex Buffers.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
67S373	N,J	com	Non-invert	Latch	S
67S374	N,J	com		Register	

The latch passes eight (octal) bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight (octal) bits of input data and passes it to the output on the "rising edge" of the clock.

The three state outputs are active when $\overline{OE}$ is low, and high impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the octal devices are packaged in the popular 20 Pin Skinny DIP.™

Function Tables

373 Octal Latch

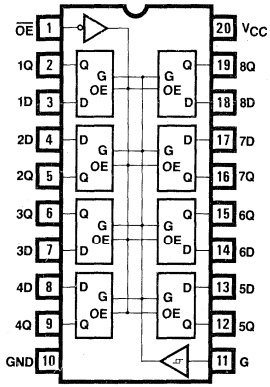
$\overline{OE}$	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

374 Octal Register

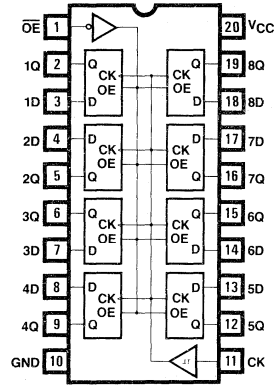
$\overline{OE}$	CK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Logic Symbols

373 Octal Latch



374 Octal Register



Monolithic Memories

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
T_A	Operating free air temperature	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			50	μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 32mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −6.5mA	2.4	3.1		V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50	μA
I_{OZH}			V_O = 2.4V			50	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX,		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S373		105	160	mA
			S374		90	140	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S373 MIN	S373 TYP	S373 MAX	S374 MIN	S374 TYP	S374 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			5	9				ns
t_{PHL}				9	13				ns
t_{PLH}	Clock/Enable to output delay			7	14		8	15	ns
t_{PHL}				12	18		11	17	ns
t_{PZL}	Output Enable delay			11	18		11	18	ns
t_{PZH}				8	15		8	15	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	12		7	12	ns
t_{PHZ}				6	9		5	9	ns
t_w	Width of Clock/Enable	High	6			6			ns
		Low	7.3			7.3			
t_{su}	Setup Time		0↓			5↑			ns
t_h	Hold Time		10↓			2↑			

9

Octal Latches, Octal Registers With Inverting, 32 mA Outputs

67S378 67S382

Features/Benefits

- **Inverting Outputs**
- **32 mA IOL**
- **3-State Outputs Drive Bus Lines**
- **20 Pin Skinny DIP™ Saves Space**
- **8 Bits Matches Byte Boundaries**
- **Hysteresis Improves Noise Margin**
- **Low Current PNP Inputs Reduce Loading**
- **Ideal for Microprocessor Interface**

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA, also inverting outputs instead of the standard non-inverting outputs.

The higher I_{OL} is intended for upgrading systems which presently satisfy 32 mA requirements with SN54/74365, 366, 367, 368, Hex Buffers. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-Bit Slice to an active low bus.

The latch passes eight (octal) bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight (octal) bits of input data and passes it to the output on the "rising edge" of the clock.

The three state outputs are active when $\overline{OE}$ is low, and high impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the octal devices are packaged in the popular 20 Pin Skinny DIP.™

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
67S382	N,J	com	Invert	Latch	S
67S378	N,J	com		Register	

Function Tables

382 Octal Latch (Inverting)

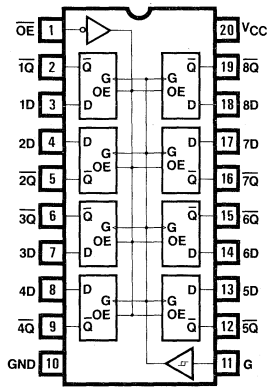
$\overline{OE}$	G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

378 Octal Register (Inverting)

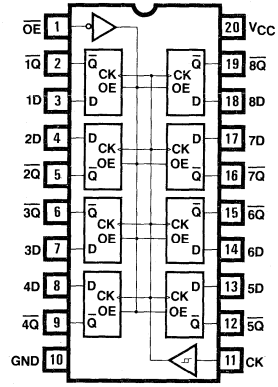
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

Logic Symbols

382 Octal Latch (Inverting)



378 Octal Register (Inverting)



Monolithic Memories

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
T_A	Operating free air temperature	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			50	μA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 32mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −6.5mA	2.4	3.1		V
I_{OZL}	Off-state output current	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50	μA
I_{OZH}			V_O = 2.4V			50	μA
I_{OS}	Output short-circuit current *	V_{CC}		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S382		105	160	mA
			S378		90	140	

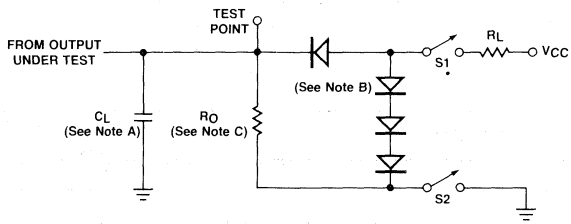
*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

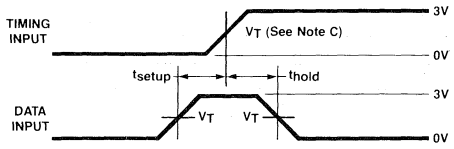
SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	S382 MIN	S382 TYP	S382 MAX	S378 MIN	S378 TYP	S378 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			9	18				ns
t_{PHL}				5	16				ns
t_{PLH}	Clock/Enable to output delay			12	22		11	20	ns
t_{PHL}				7	20		8	18	ns
t_{PZL}	Output Enable delay			11	20		11	20	ns
t_{PZH}				8	17		8	17	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	16		7	16	ns
t_{PHZ}				6	13		5	13	ns
t_w	Width of Clock/Enable	High	6			6			ns
		Low	7.3			7.3			
t_{su}	Setup Time		0↓			5↑			ns
t_h	Hold Time		10↓			2↑			

9

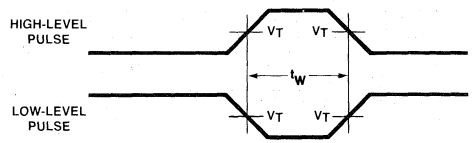
Test Load



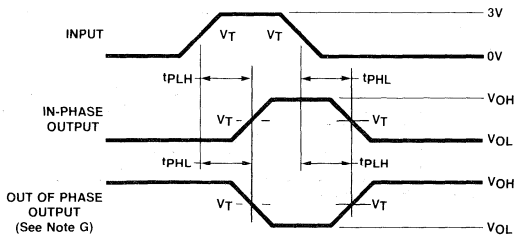
Test Waveforms



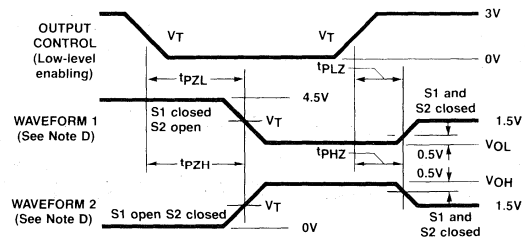
Setup and Hold



Pulse Width



Propagation Delay



Enable and Disable

NOTES: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

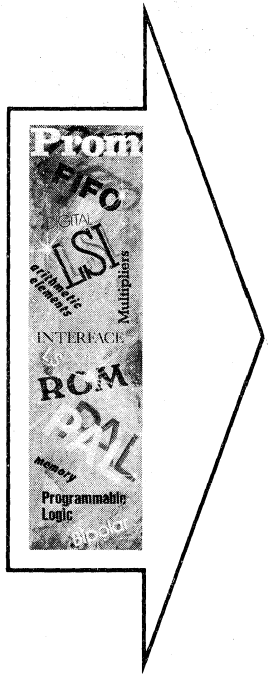
C. For Series 54/74S, 57/67S, R_O = 1K, V_T = 1.5V
For Series 54/74LS and 57/67LS, R_O = 5K, V_T = 1.2V excepting 57/67LS300, 301, 304
For Series 54/74LS300, 301, 304 R_O = 5K, $V_T = V_{T+}$ = 1.7V for low to high input transition
For Series 54/74LS300, 301, 304 R_O = 5K, $V_T = V_{T-}$ = 0.9V for high to low input transition

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50Ω and:
For Series 54/74S and 57/67S, $t_R \leq 2.5$ ns $t_F \leq 2.5$ ns
For Series 54/74LS and 57/67LS, and PALs, $t_R \leq 15$ ns $t_F \leq 6$ ns

G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.



Setup Time

Setup time, t_{su}

The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Input clamp voltage, V_{IC}

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Negative-going threshold voltage, V_T

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

Positive-going threshold voltage, V_{T+}

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

Truth Table Explanations

H	=	high level (steady-state)
L	=	low level (steady-state)
↑	=	transition from low to high level
↓	=	transition from high to low level
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a..h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output.

Clock Frequency

Maximum clock frequency, f_{max}

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

Current

High-level input current, I_{IH}

The current into * an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}

The current into * an output with input conditions applied that according to the product specification will establish a high level at the output.

High-level output current, I_{CEX}

The high-level leakage current of an open collector output.

Low-level input current, I_{IL}

The current into * an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}

The current into * an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}

The current into * an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}

The current into * an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{CC}

The current into * the V_{CC} supply terminal of an integrated circuit.

*Current out of a terminal is given as a negative value.

Hold Time

Hold time, t_h

The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, t_{PZH} (or low level, t_{PZL})

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, t_{PZX}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, t_{PHZ} (or low level, t_{PLZ})

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

Output disable time (of a three-state output) from high or low level, t_{PXZ}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

t_{EA} is the output enable access time of memory devices. t_{ER} is the output disable (enable recovery) time of memory devices.

Propagation Time

Propagation delay time, t_{PD}

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, t_{PLH}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, t_{PHL}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{AA} is the address (to output) access time of memory devices.

Pulse Width

Pulse width, t_w

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Programming Input Formats

MMI can program your ROM or PROM from input data in any of several types: truth table, punched cards, paper tape or pre-programmed ROM or PROM. However, the preferred input data for PROMs is paper tape and for ROMs punched cards.

Truth Table Inputs

Devices are programmed at our facility from MMI truth table forms (available on request). For customers desiring to make their own forms, examples are shown below:

4-BIT OUTPUT

WORD NUMBER	PIN	OUTPUTS 10	11	12	13
		O_4	O_3	O_2	O_1
0		H	H	H	L
1		L	H	L	H
.		.	.	.	.
.		.	.	.	.
255		L	H	H	H

8-BIT OUTPUT

WORD NUMBER	PIN	OUTPUTS 17	16	15	14	13	11	10	9
		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0		H	H	H	L	H	L	H	H
1		L	H	L	H	L	H	L	H
.		.	.	.	.	.	.	.	.
.		.	.	.	.	.	.	.	.
511		L	H	H	H	H	H	H	L

NOTE: A high voltage on the data out lines is signified by an "H." A low voltage on the data out lines is signified by an "L." The word number assumes positive logic on the address pins, so for example, word 1023 = HHHHHHHHHH.

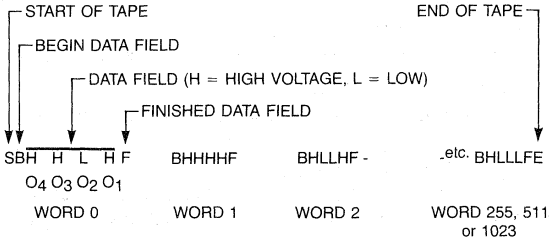
Paper Tape Format Inputs

Truth tables can also be sent to MMI in an ASCII tape in either a 7 or 8 level format. Send information air mail or TWX 910-339-9224. The tape reading equipment at MMI only recognizes ASCII characters S, B, H, L, F and E and interprets them respectively as Start, Begin a word, High data, Low data, Finish a word, and End of tape. All other characters such as carriage returns, line feeds, etc. are ignored so that comments and spaces may be sent in the data field to improve readability. Comments, however, should not use the characters S, B, H, L, F, E. Word addresses must begin with zero and count sequentially to word 31, 255, 511 or 1023 respectively.

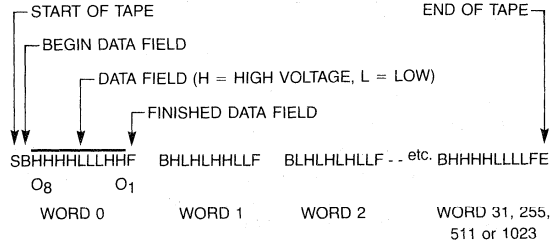
In order to assist the machine operator in determining where the heading information stops and the data field begins, 25 bell characters or rubout characters should precede the start of the truth table. Any type of 8 level paper tape (mylar, fanfold, etc.) is acceptable. Channel 1 is the most significant bit and channel 8 (parity) is ignored. Sprocket holes are located between channels 3 and 4. Note that the order of the outputs between characters B and F is O_4, O_3, O_2, O_1, not O_1, O_2, O_3, O_4.

A typical list of characters and their machine interpretations is shown below:

4-BIT OUTPUT



8-BIT OUTPUT



The required heading information at the beginning of the tape is as follows:

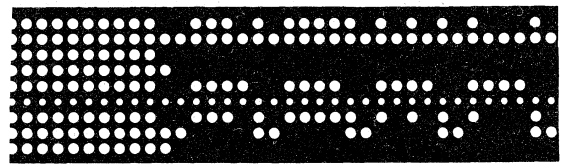
CUSTOMER'S NAME AND PHONE _____
CUSTOMER'S TWX NUMBER _____
PURCHASE ORDER NUMBER _____
MMI PART NUMBER _____
CUSTOMER SYMBOLIZED PART NUMBER _____
TRUTH TABLE NUMBER _____
NUMBER OF TRUTH TABLES _____
TOTAL NUMBER OF PARTS _____
NUMBER OF PARTS OF EACH TRUTH TABLE _____
25 BELL OR RUBOUT CHARACTERS _____

An example is shown below for a 256 x 4 PROM (6300)

SCOTT ELECTRONICS 408 426-6134
TWX 911-338-9225
PO142
6300
0431
12
1
3
3

SBLLLHF BLLLLF BLHLHF BLHHHF BLLHHF BHHHHF BLLLHF BLHLHF BLLLLF
BLLLLF BLHLHF BLLHHF BHHHLF BHHLLF BLLHHF BHHLLF BLLHHF BLHLHF

8 level
TWX



ROM Programming Punched Card

ROMs can be programmed using several input methods. These are truth table, punched cards in the format shown below, paper tape in the same format as cards, and paper tape in the ASCII BHLF format of the equivalent PROM.

Punched Card or Tape Input

First card or line (80 columns max.): enter Company Name, Part Number, Data, Number of "L's" in Pattern.
(Free Form Entry: no commas; Paper Tape Format: terminate each line with carriage return and linefeed).

Hexadecimal Format

In this format the heading required is identical to the BHLF format but the data is different. Instead of an "S," the hexadecimal data begins with the SOH character (control A). The data is then represented by the hexadecimal character (0-9 and A-F) which represents the output data of address 0, followed by a space. Next comes the output data of address 1 followed by a space, etc. The character ETX (control C) is used to end the data. Carriage return and the line feed may be included to format the data when the tape is printed.

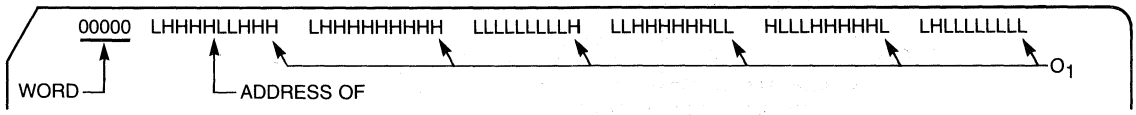
CARD 1

COMPANY NAME CX 1816—2052 7—12—70 L = 796

2nd Card Or Line thru Last (80 Columns Max.)
ENTER WORD ADDRESS OF FIRST DATA FIELD IN COLUMNS 1 THRU 5

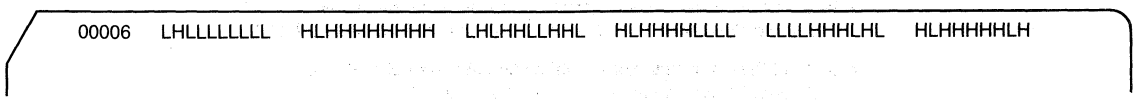
Enter First Data Field	(O_{10}—O_1) in Columns 8 thru 17
Enter Second Data Field	(O_{10}—O_1) in Columns 19 thru 28
Enter Third Data Field	(O_{10}—O_1) in Columns 30 thru 39
Enter Fourth Data Field	(O_{10}—O_1) in Columns 41 thru 50
Enter Fifth Data Field	(O_{10}—O_1) in Columns 52 thru 61
Enter Sixth Data Field	(O_{10}—O_1) in Columns 63 thru 72

CARD 2

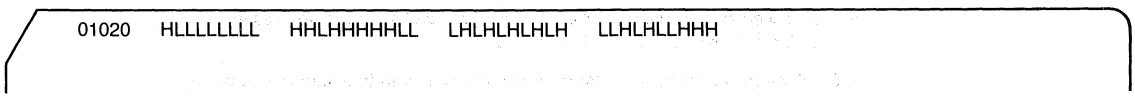


NOTE: Output 1 (O_1) is always in cols. 17,28,39,50,61,72

CARD 3



LAST CARD



NOTES:

1. Leading edge zeroes in the word number may be eliminated. Columns 73 thru 80 are for comments.
2. Regardless of the number of outputs which a particular ROM has, the data for a specific output always goes in a specific column.

Output 1 (01)	Columns 17, 28, 39, 50, 61, 72
Output 2 (02)	Columns 16, 27, 38, 49, 60, 71
Output 3 (03)	Columns 15, 26, 37, 48, 59, 70
Output 4 (04)	Columns 14, 25, 36, 47, 58, 69
Output 5 (05)	Columns 13, 24, 35, 46, 57, 68
Output 6 (06)	Columns 12, 23, 34, 45, 56, 67
Output 7 (07)	Columns 11, 22, 33, 44, 55, 66
Output 8 (08)	Columns 10, 21, 32, 43, 54, 65
Output 9 (09)	Columns 9, 20, 31, 42, 53, 64
Output 10 (10)	Columns 8, 19, 30, 41, 52, 63

3. 0 and 1 may replace L and H, but the customer must define for MMI whether 0 = L or 0 = H.

Application Notes

PROMS

- **PROM card simplifies computer diagnosis**
  Shlomo Waser, Computer Design, January 1977
- **Registered PROMs Impact Computer Architecture**
  John Birkner

PAL

- **Reduce random-logic complexity by using arrays of fuse-programmable circuits**
  John Birkner, Electronic Design, August 16, 1978
- **High speed/low cost fuse link arrays compete with TTL 74S/LS**
  John Birkner, WESCON '78
- **Synthesis of stable output state sequencers**
  Bill Black, WESCON '78
- **PALs: Programmable logic functions help minimize hardware**
  John Birkner, WESCON '79

FIFO

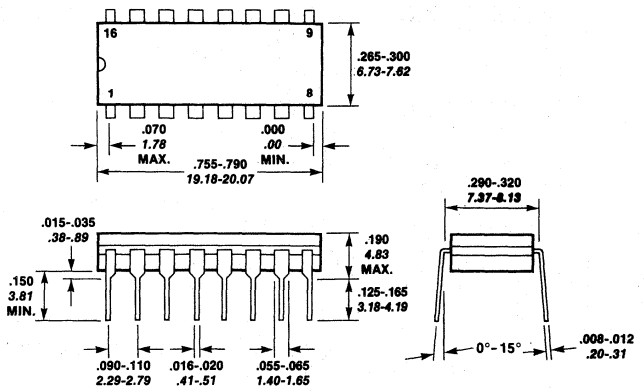
- **First-in First-out Memories**
  Operations and Applications

MULTIPLIERS

- **Real-time processing gains ground with fast digital multiplier**
  Shlomo Waser and Allen Peterson, Electronics, September 29, 1977
- **State-of-the-art in high speed arithmetic integrated circuits**
  Shlomo Waser, Computer Design, July 1978
- **Dedicated multiplier ICs speed up processing in fast computer systems**
  Shlomo Waser, Electronic Design, September 1978
- **High-speed monolithic multipliers for real-time digital signal processing**
  Shlomo Waser, Computer, October 1978
- **Medium-speed multipliers trim cost, shrink bandwidth in speed transmission**
  Shlomo Waser and Dr. Allen Peterson, Electronic Design, February 1, 1979

J16 Ceramic DIP

θ_{JA} = 75° C/W
θ_{JC} = 35° C/W



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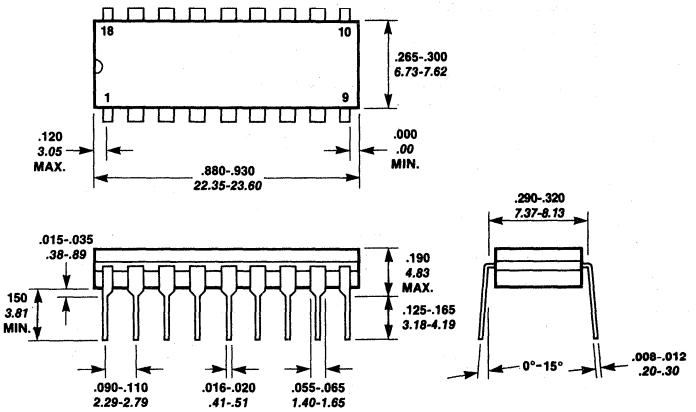
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

J18 Ceramic DIP

θ_{JA} = 75° C/W
θ_{JC} = 35° C/W



UNLESS OTHERWISE SPECIFIED:
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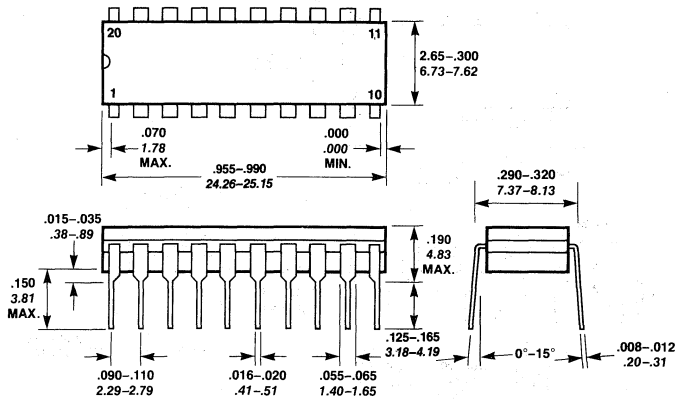
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

10

J20 Ceramic DIP

θ_{JA} = 75°C/W
θ_{JC} = 35°C/W



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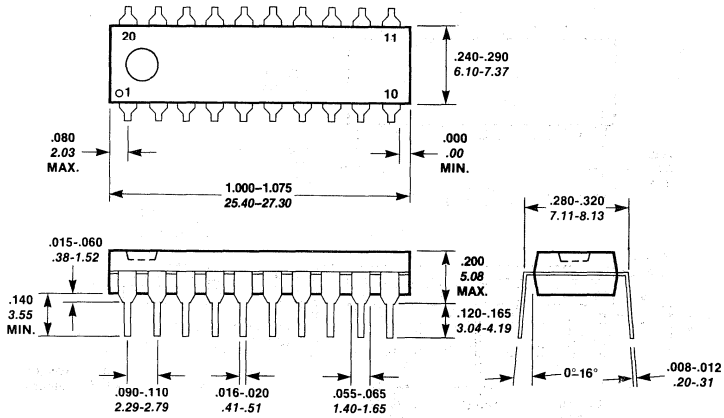
N20 Plastic Kool DIP™

θ_{JA} = 75°C/W
θ_{JC} = 35°C/W



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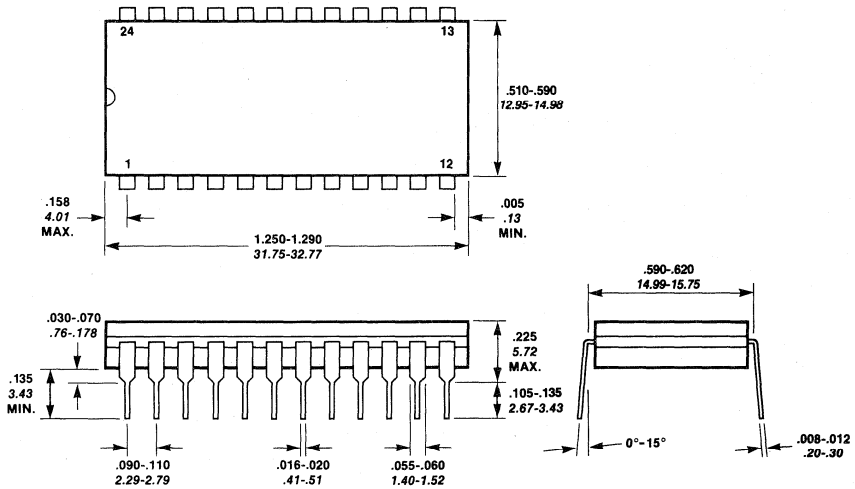
J24 Ceramic DIP

θ_{JA} = 65°C/W
θ_{JC} = 30°C/W



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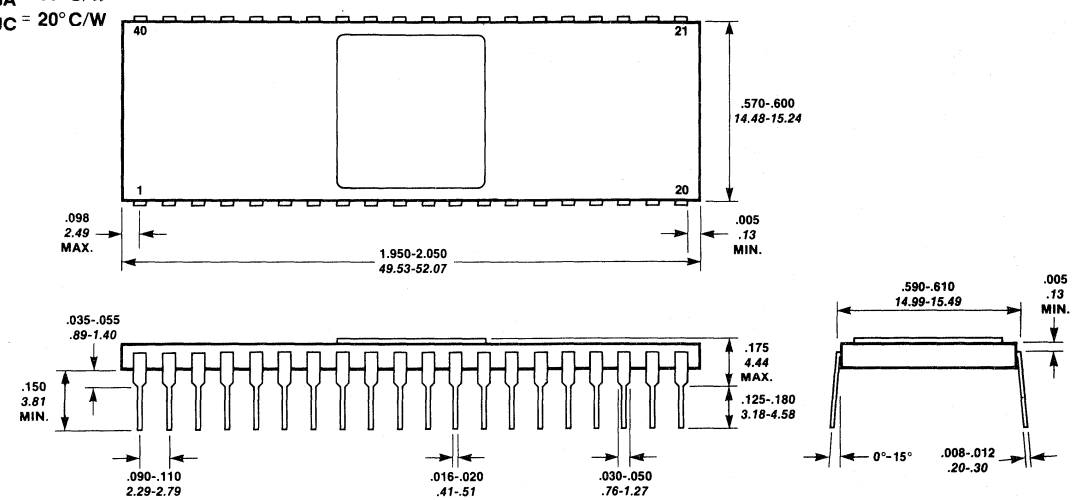
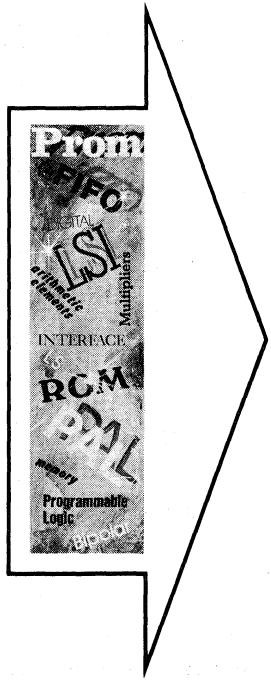
D40 Side Brazed Ceramic DIP

θ_{JA} = 55°C/W
θ_{JC} = 20°C/W



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

10



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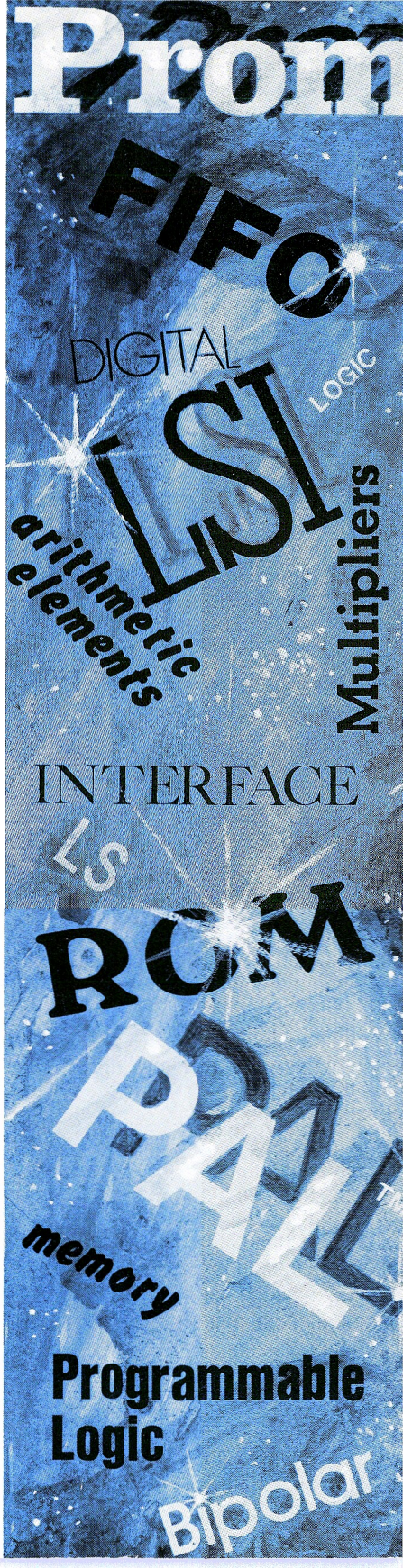

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